Sistemas Digitales
Compuertas

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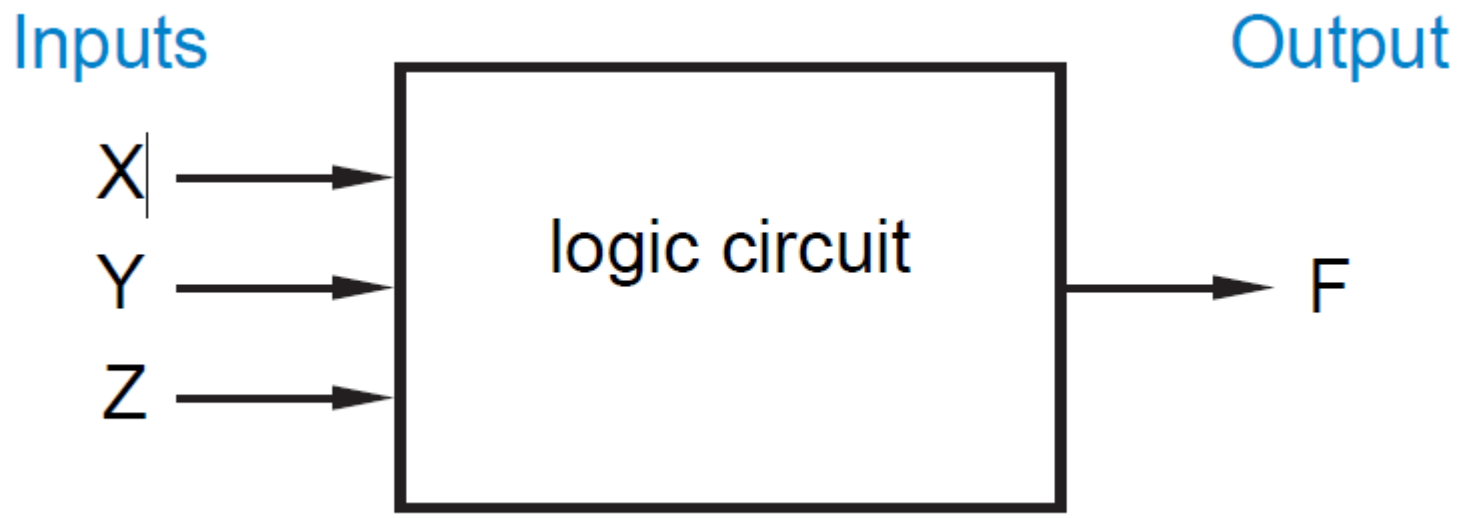
Señales Lógicas

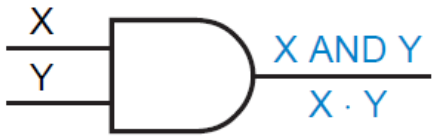
- Lógica Positiva:
  - BAJO (L): señal comprendida en el intervalo de voltaje más bajo, se interpreta como 0 lógico
  - ALTO (H): señal comprendida en el intervalo de voltaje más alto, se interpreta como 1 lógico
- Lógica Negativa:
  - BAJO (L): se interpreta como 1 lógico
  - ALTO (H): se interpreta como 0 lógico

Circuito Digital (Lógico)



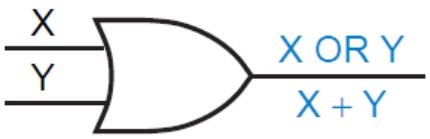
Compuertas Básicas

(a)



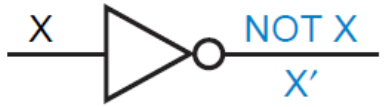
X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)



X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

(c)



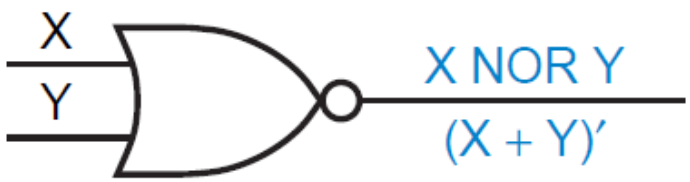
X	NOT X
0	1
1	0

Compuertas Inversoras

(a)

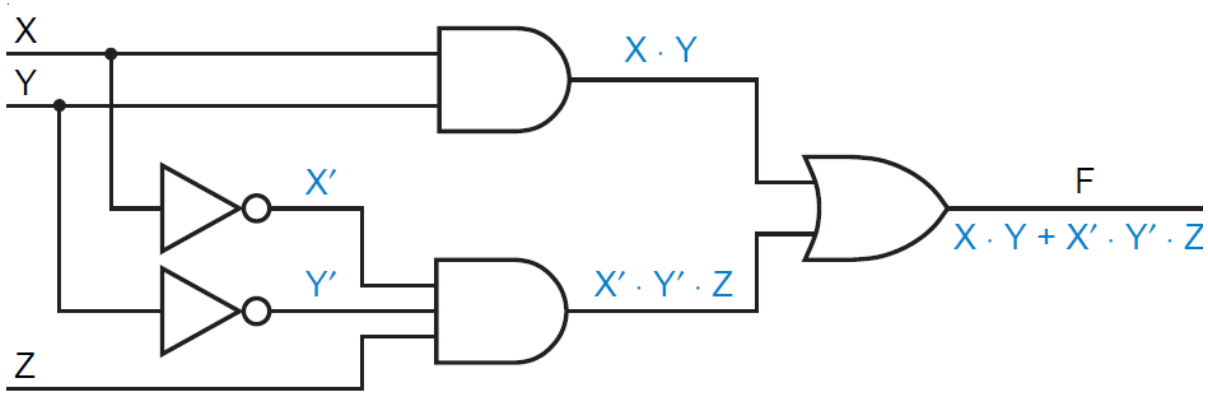
X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

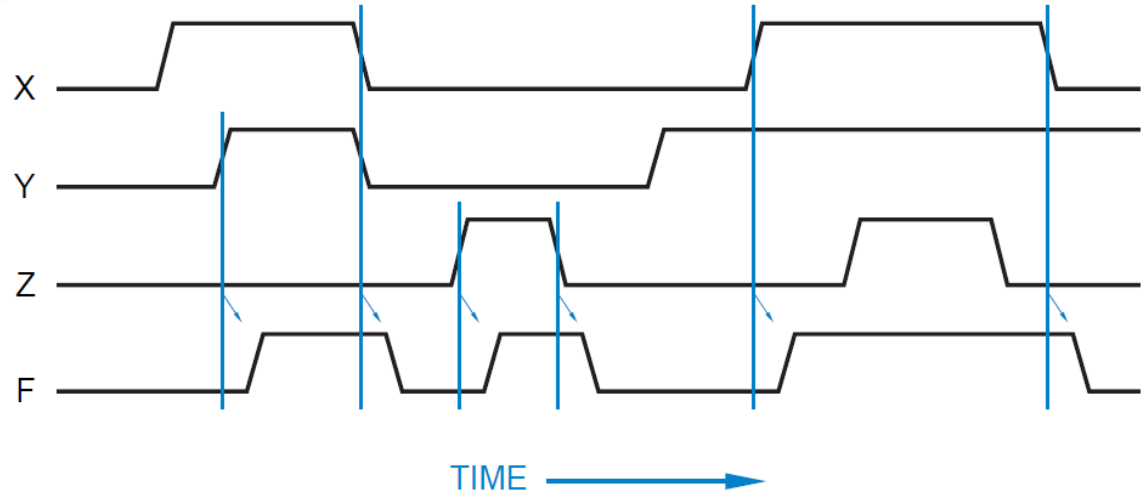
(b)



X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

Tabla de Verdad



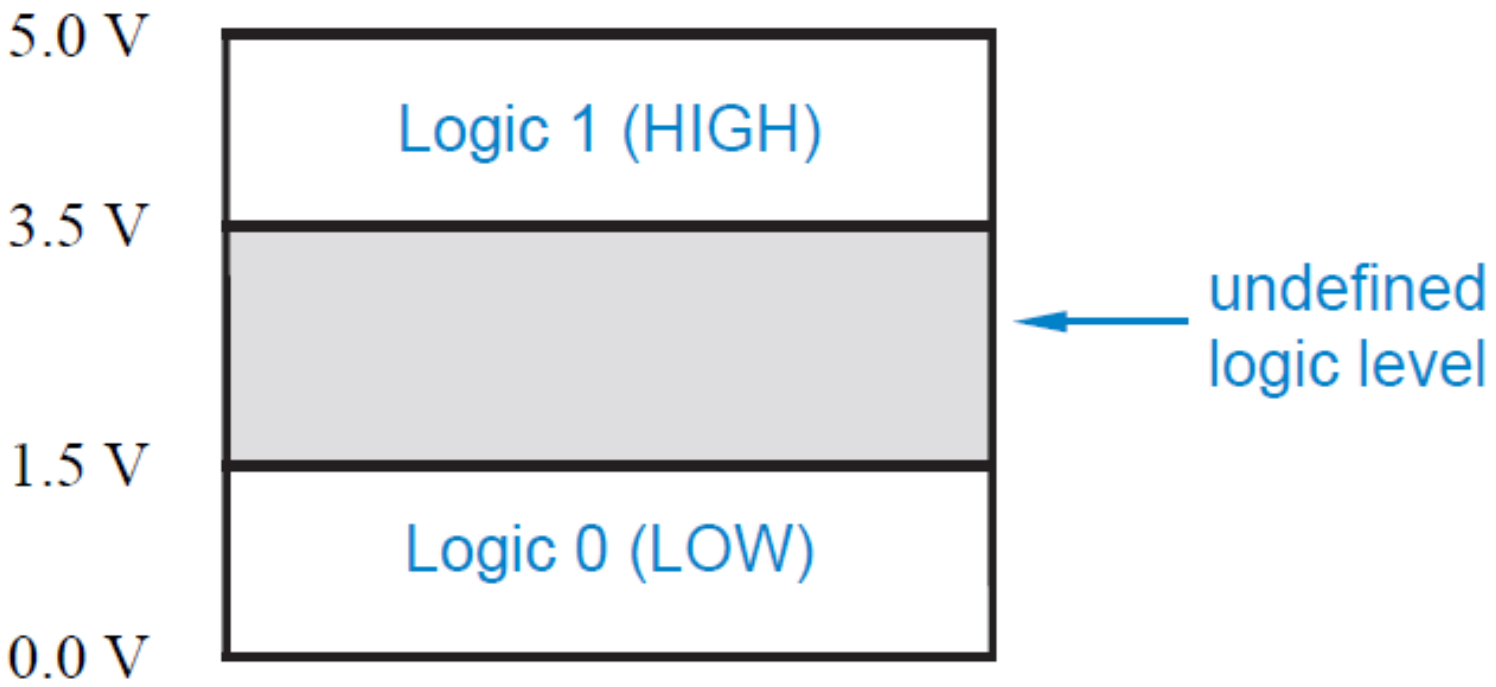


X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

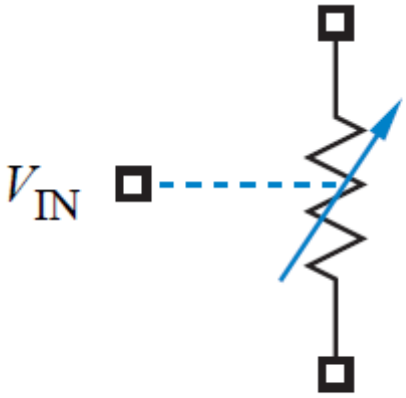
Familias Lógicas

- Una Familia Lógica es una colección de diferentes Circuitos Integrados que tiene características similares en sus entradas, salidas y circuitería interna.
- Familias más populares:
  - MOS Complementario (CMOS)
  - Lógica Transistor-Transistor (TTL)

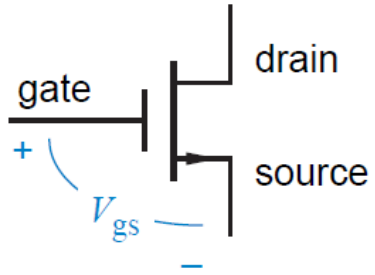
Lógica CMOS


5.0 V
Logic 1 (HIGH)
3.5 V
undefined
logic level
1.5 V
Logic 0 (LOW)
0.0 V

Transistor MOS

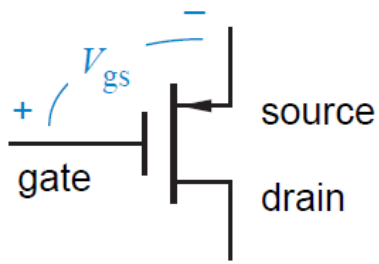


Circuit symbol for an n-channel MOS (NMOS) transistor.



Voltage-controlled resistance: increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$



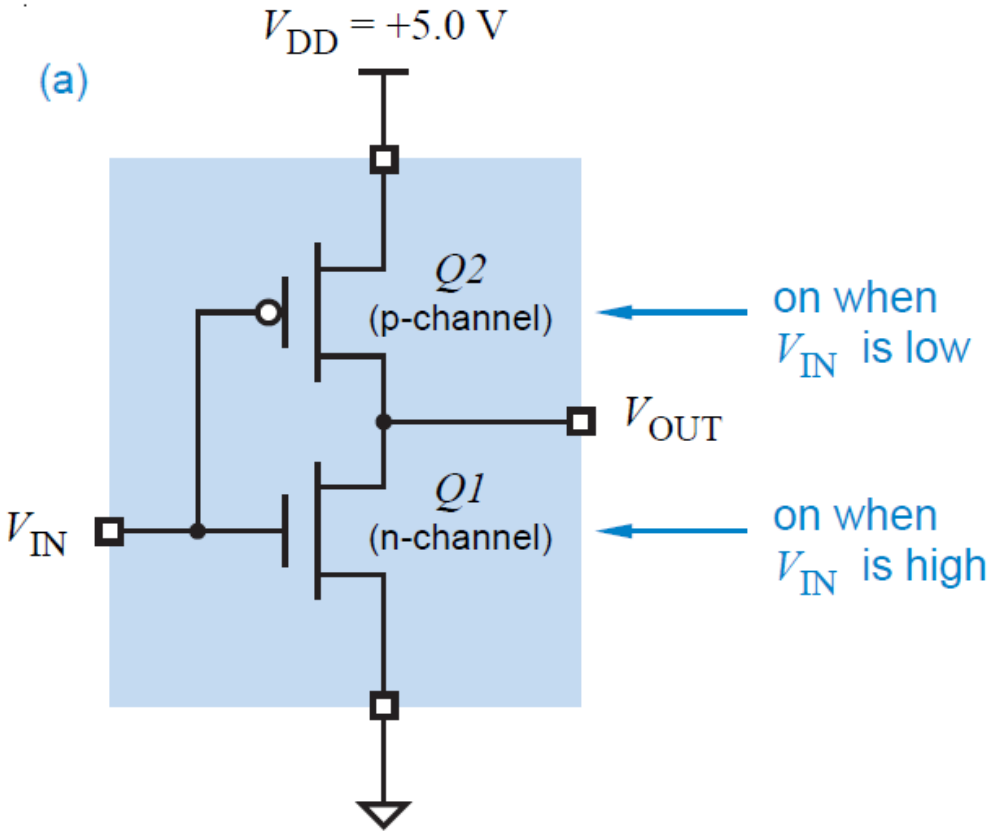
Voltage-controlled resistance: decrease V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

Circuit symbol for a p-channel MOS (PMOS) transistor.

Compuerta NOT

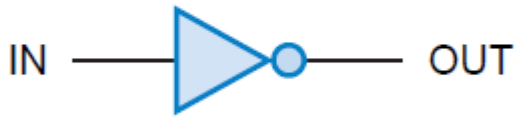
(a)



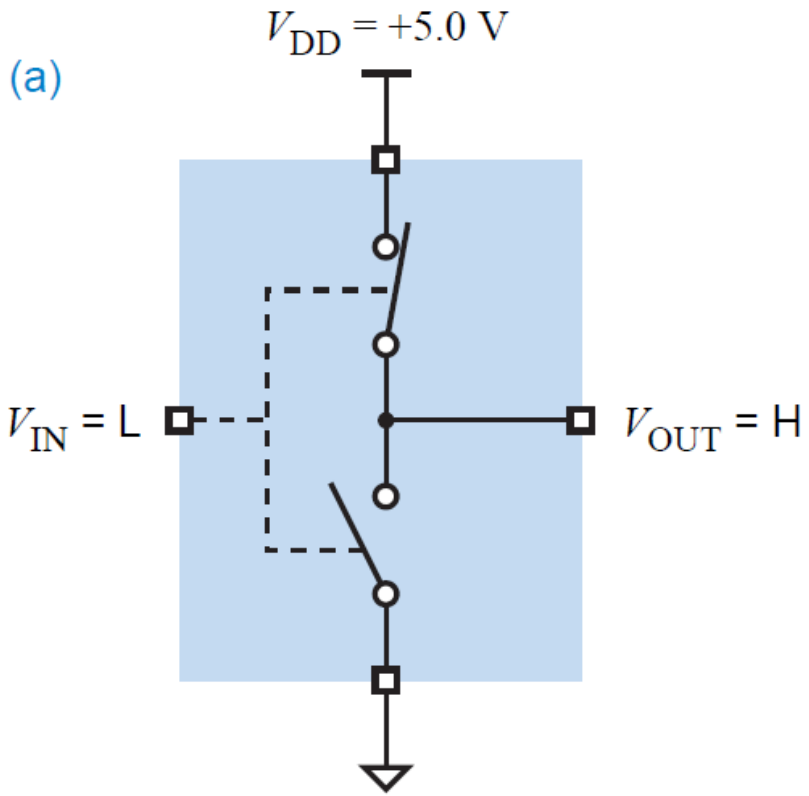
(b)

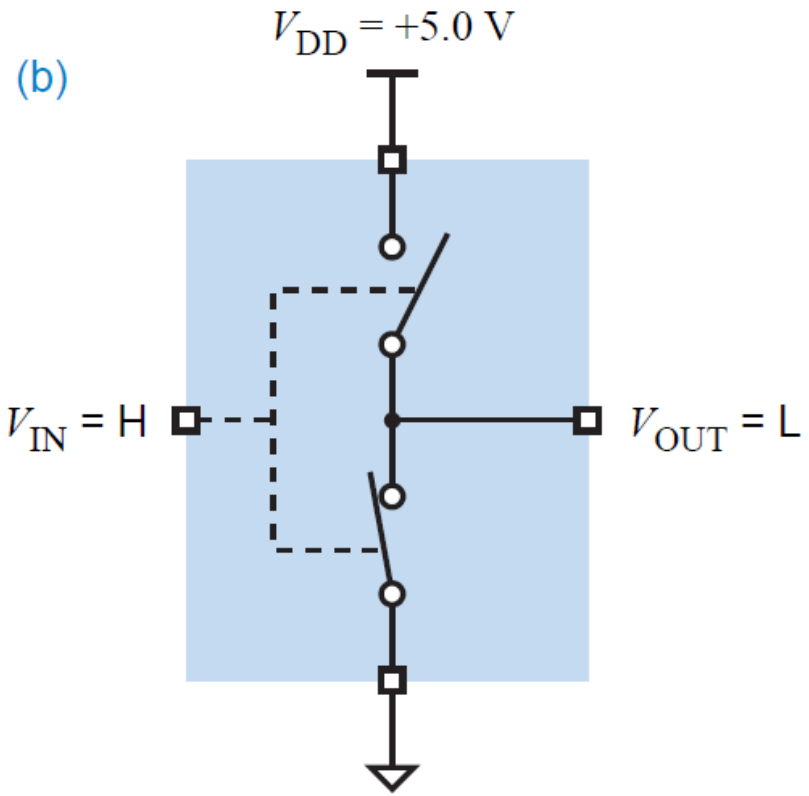
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)



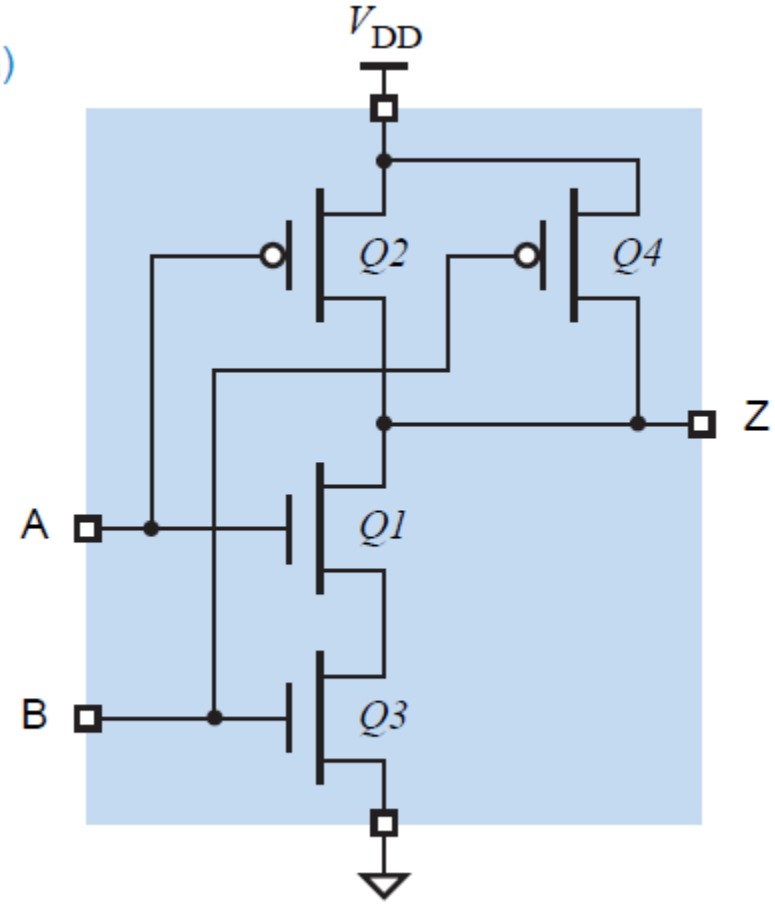
Compuerta NOT





Compuerta NAND

(a)



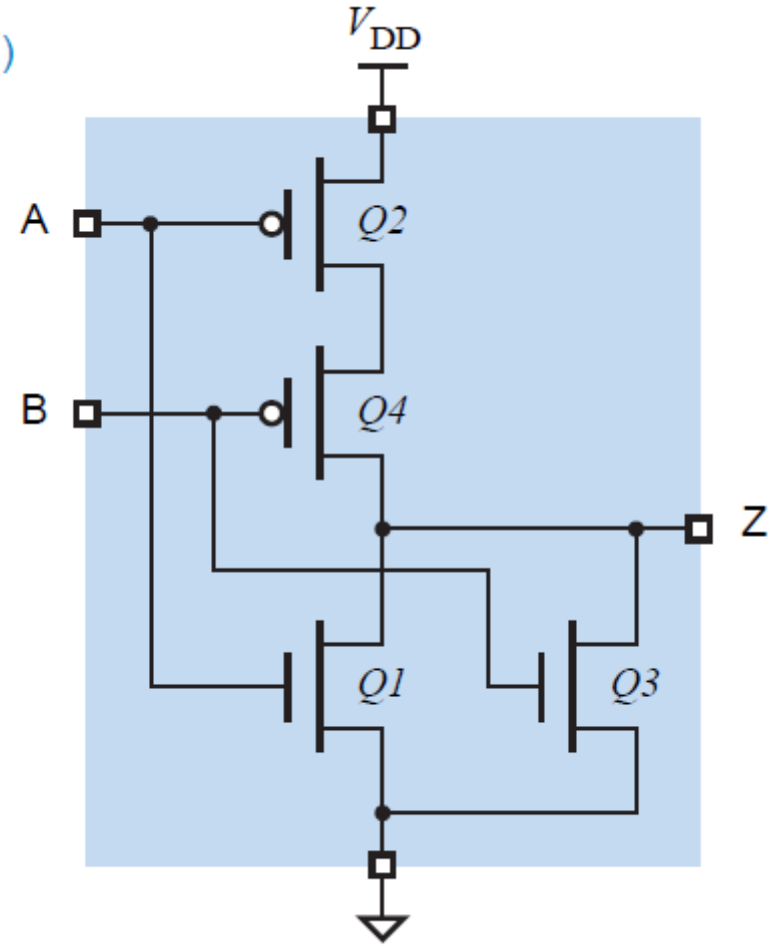
(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

(c)

Compuerta NOR

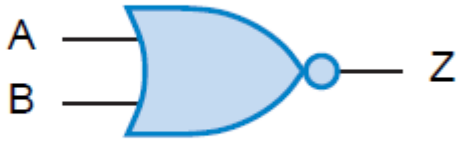
(a)



(b)

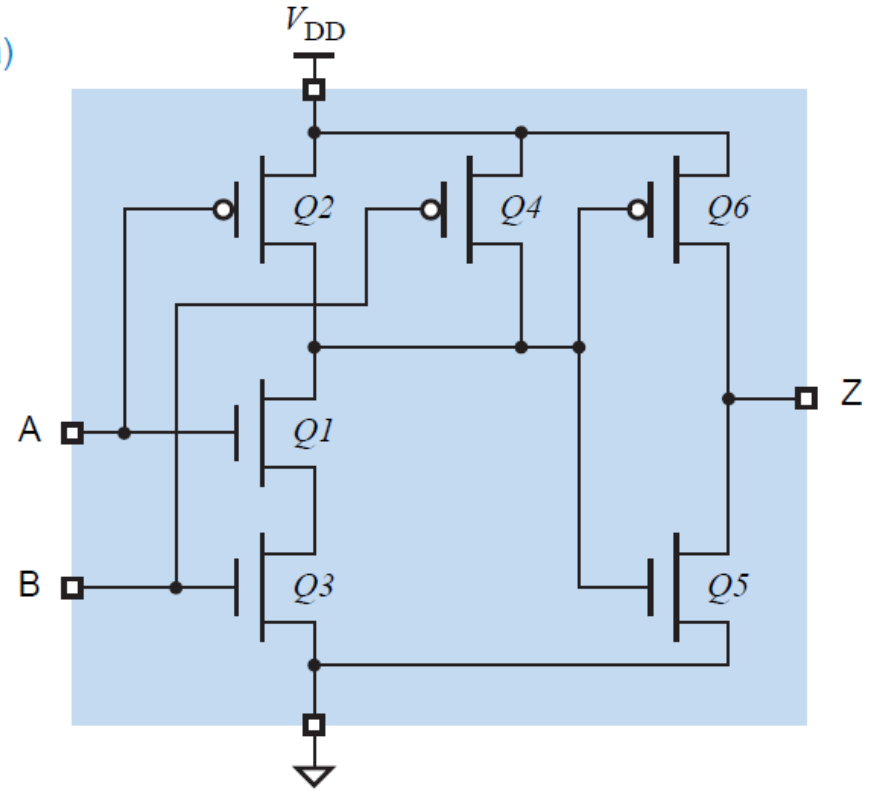
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)



Compuerta AND

(a)

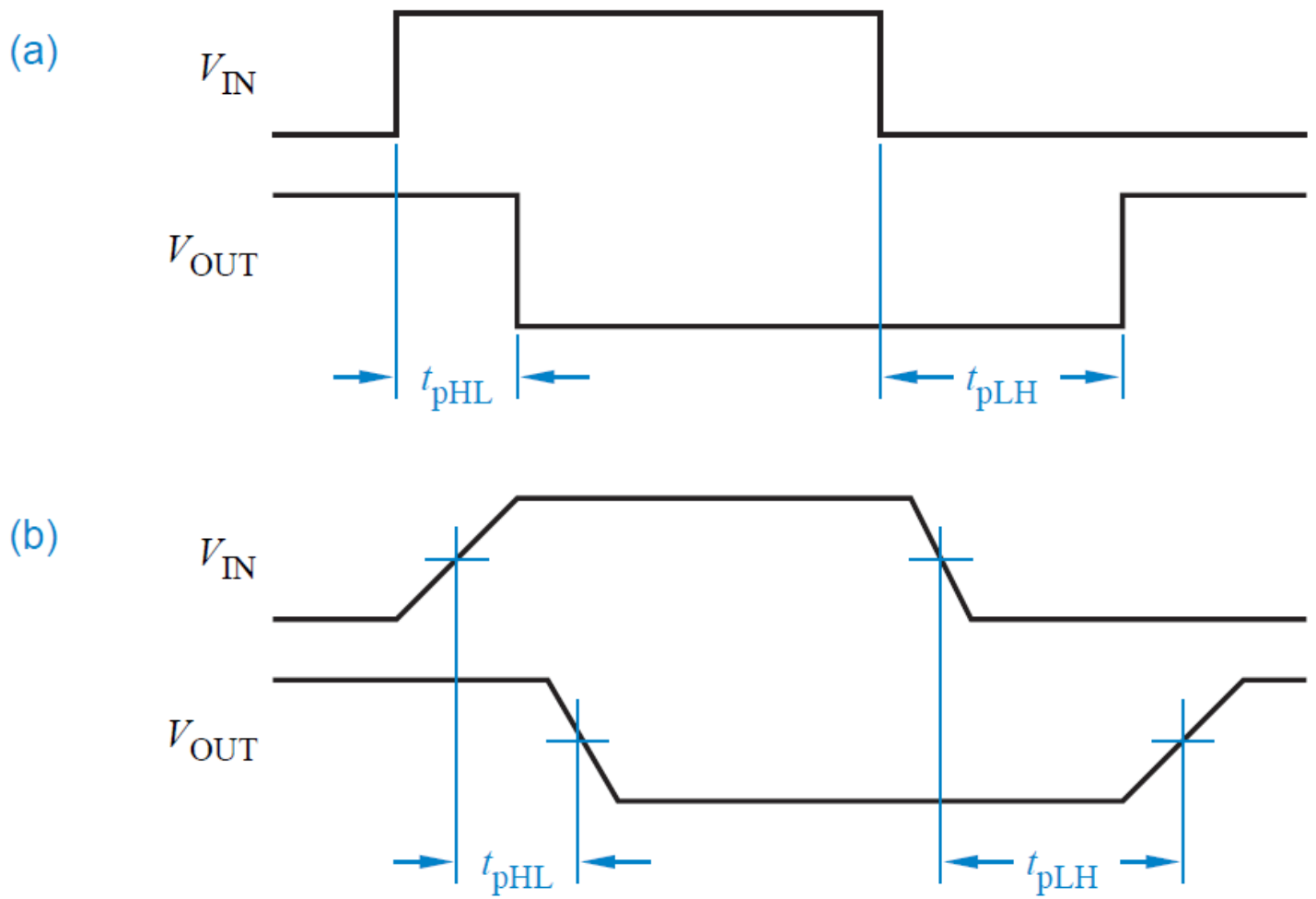


(b)

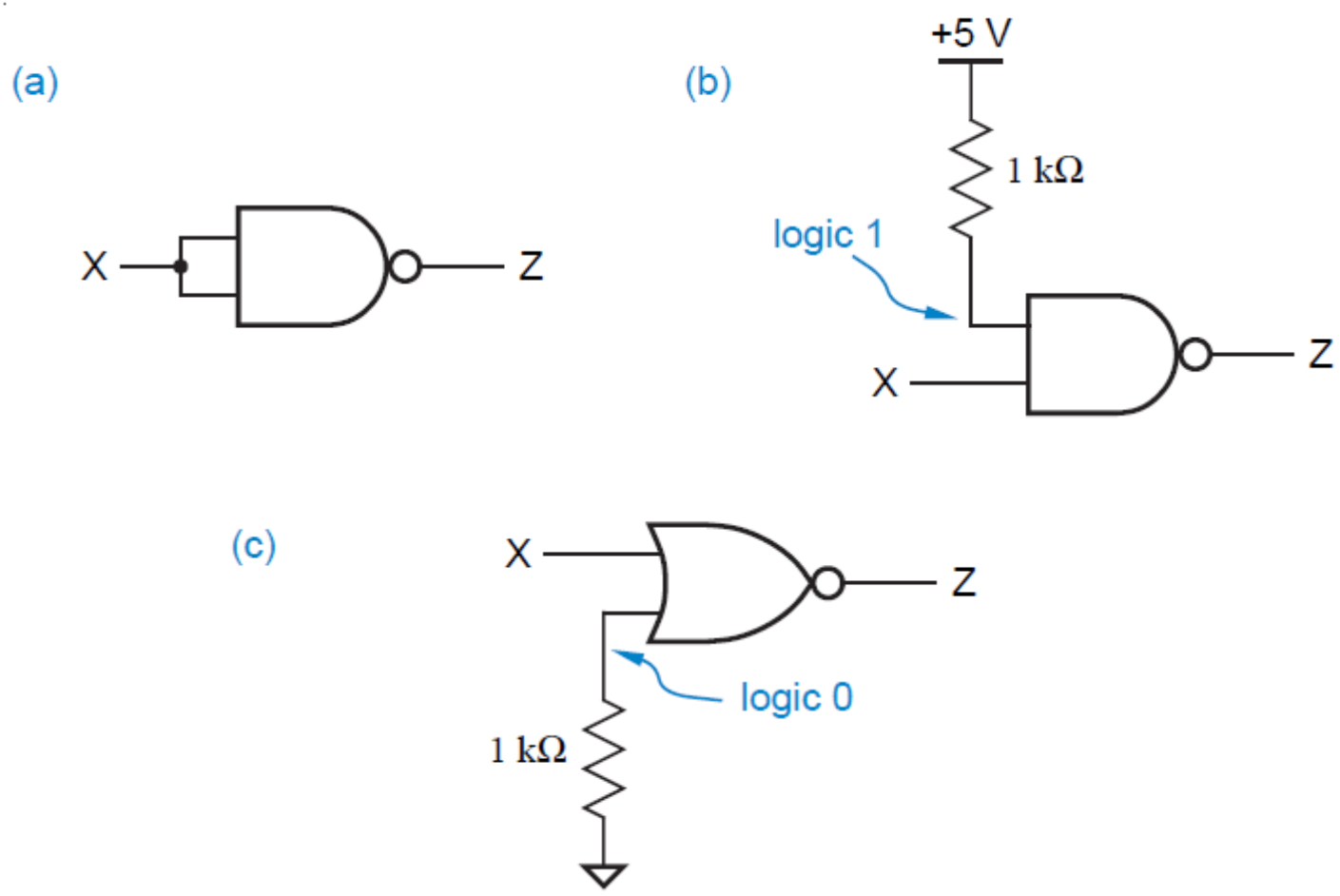
A	B	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

(c)

Retardos de Propagación

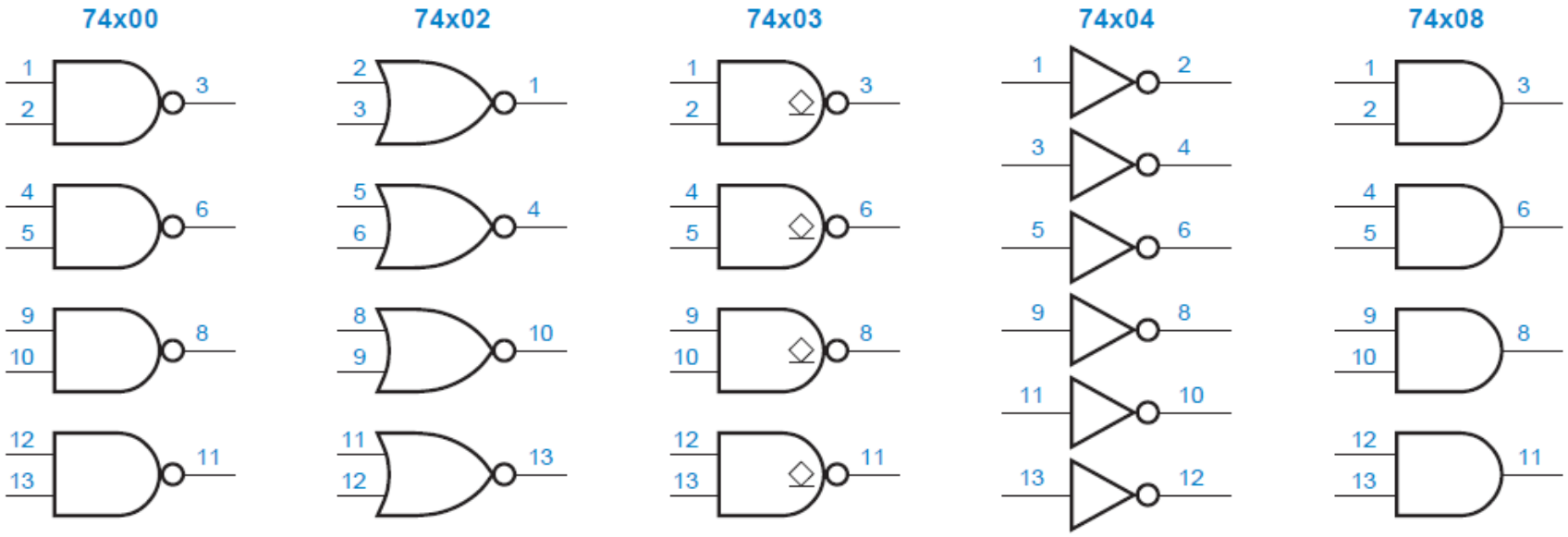


Entradas sin utilizar



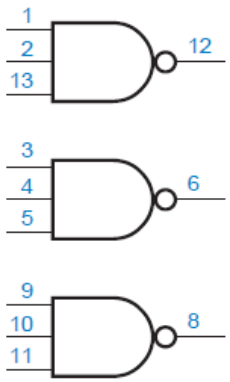
Circuitos Integrados Comerciales

- CMOS: HC, HCT, VHC, VHCT
- TTL: S, LS, AS, ALS, F

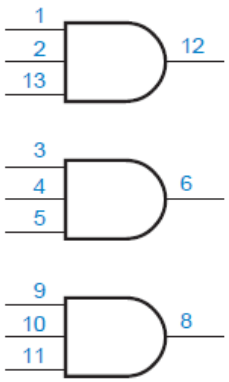


Circuitos Integrados Comerciales

74x10



74x11



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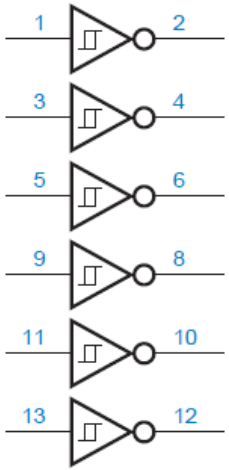
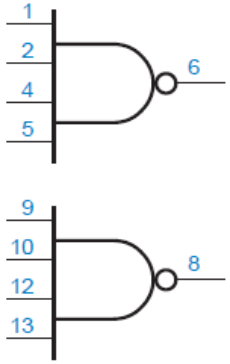


74x20



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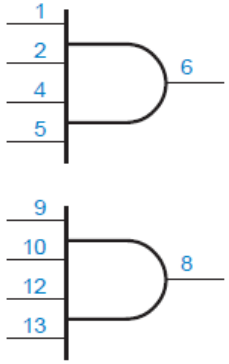

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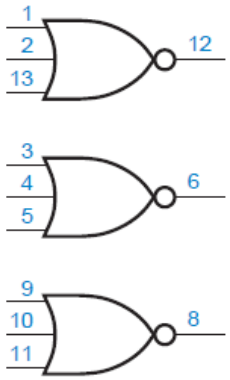

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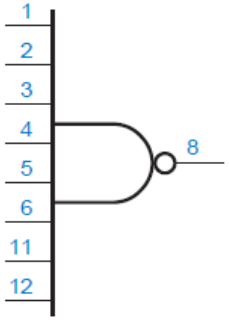

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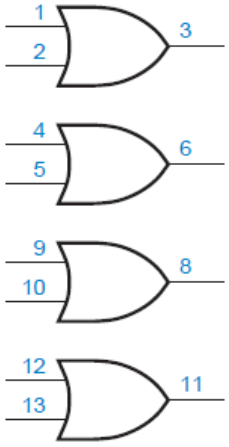

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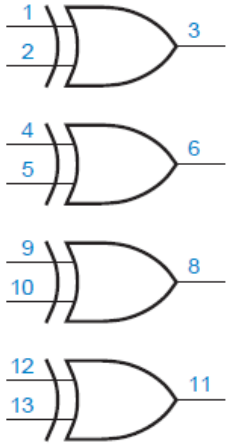

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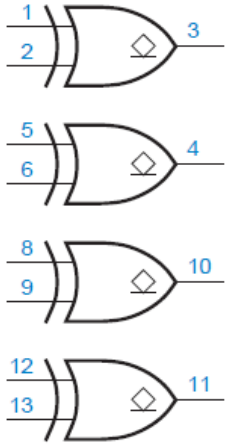

Interface TTL – CMOS