

Sistemas Digitales

Memorias

Flip-Flops

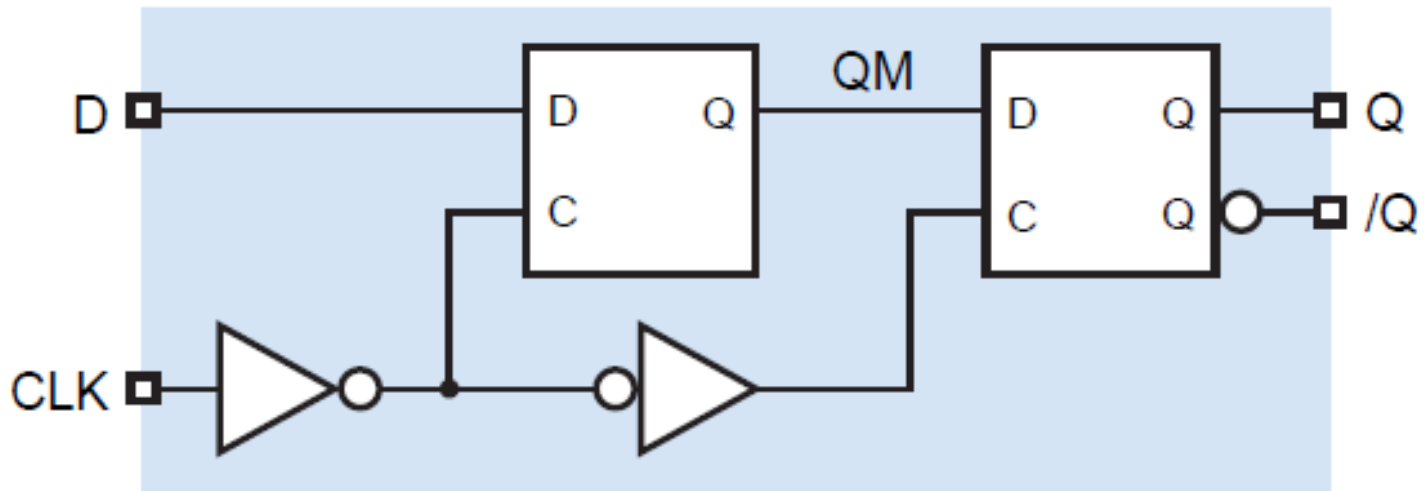
Prof. Luis Araujo

Escuela de Ingeniería Eléctrica



Flip Flop D flanco positivo(LH)

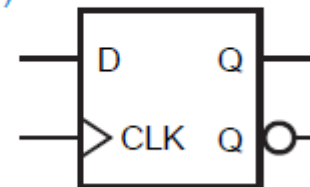
(a)



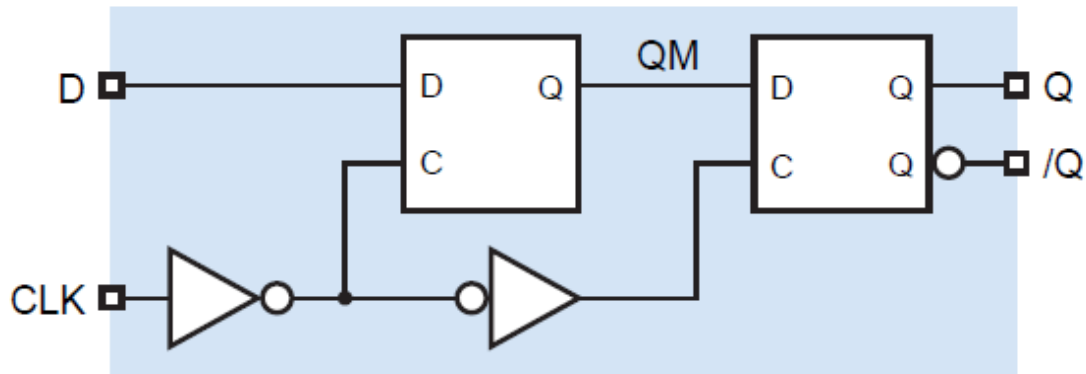
(b)

D	CLK	Q	/Q
0		0	1
1		1	0
x	0	last Q	last /Q
x	1	last Q	last /Q

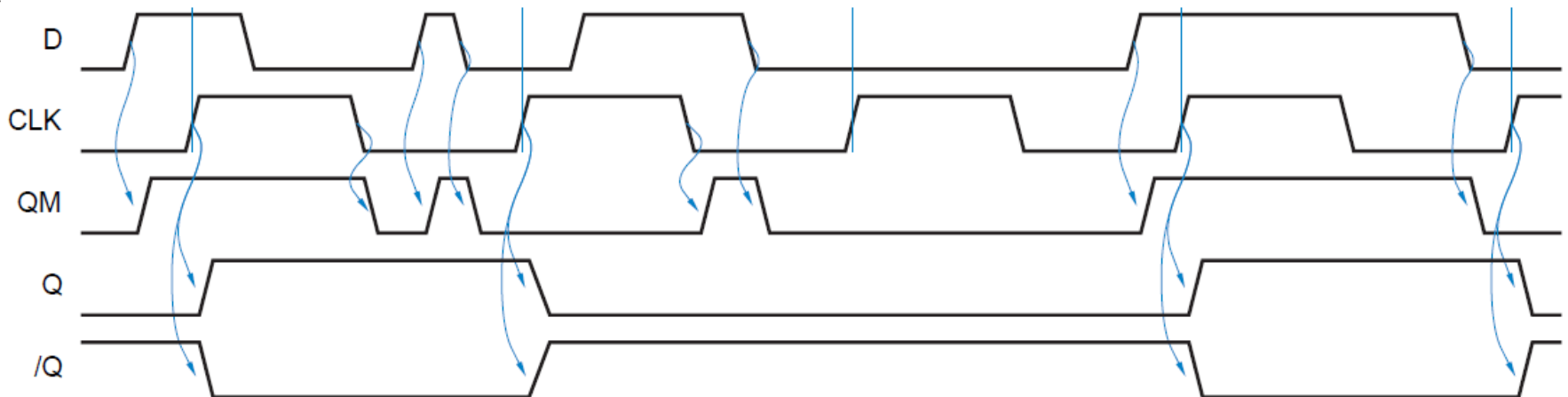
(c)



Flip Flop D

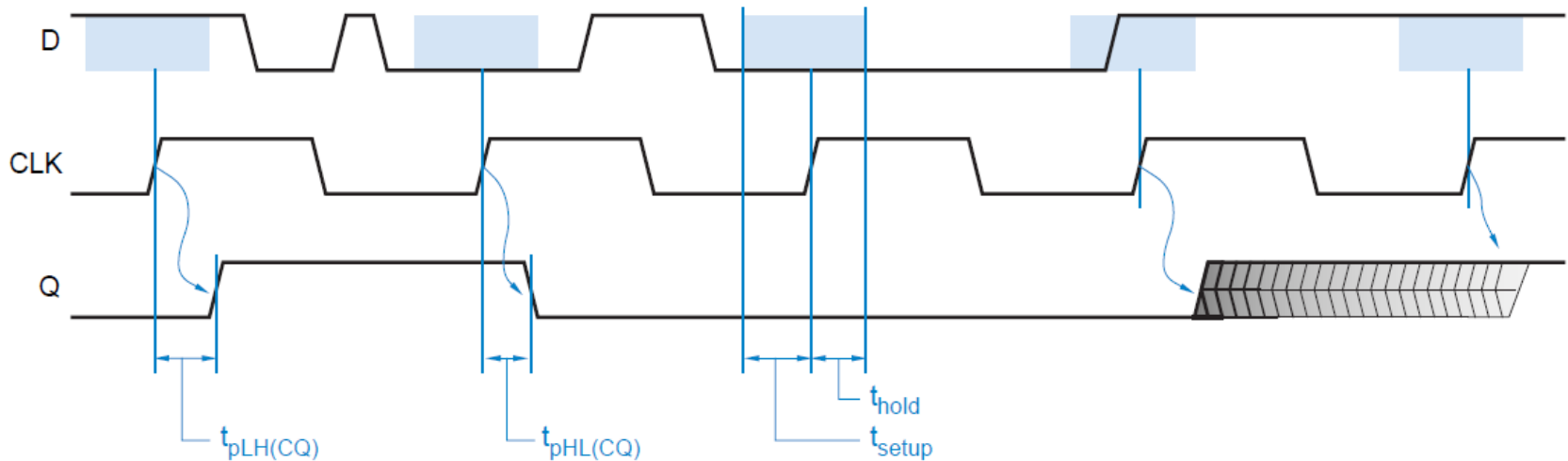


C	D	Q	/Q
1	0	0	1
1	1	1	0
0	x	last Q	last /Q

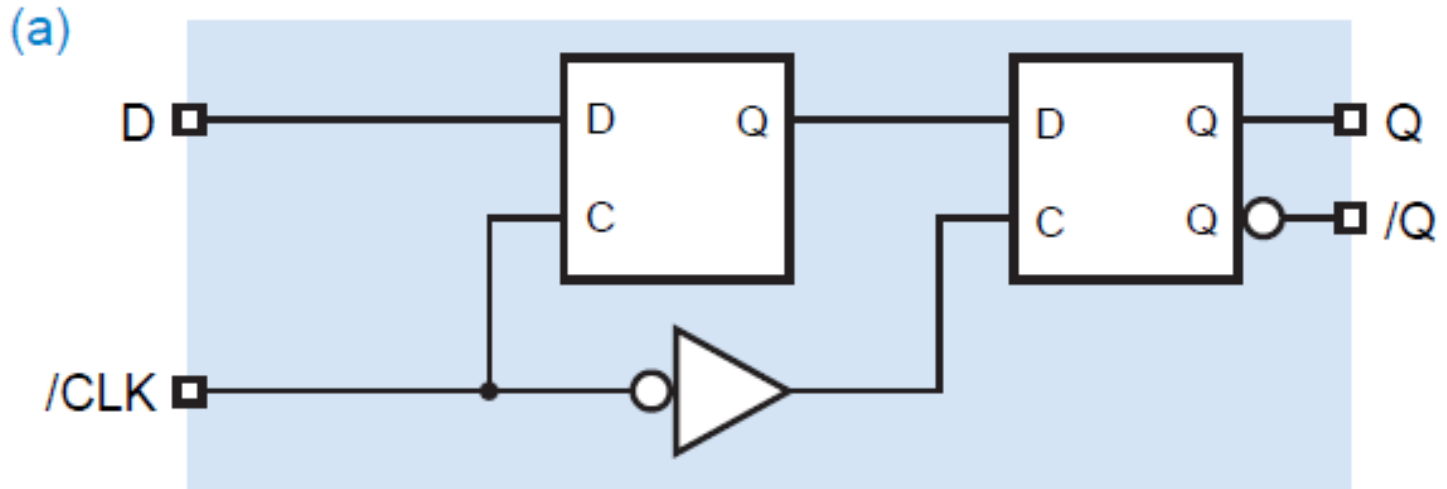


Temporización Flip Flop D

- Retardo de propagación (t_p)
 - $t_{pLH(CQ)}$, $t_{pHL(CQ)}$
- Tiempo de Establecimiento (t_{setup})
- Tiempo de Retención (t_{hold})

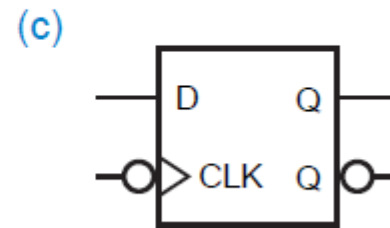


Flip Flop D flanco negativo(HL)

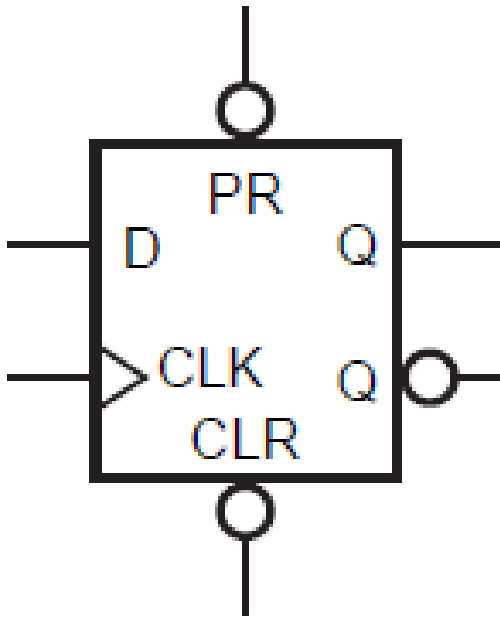




(b)

D	/CLK	Q	/Q
0		0	1
1		1	0
x	0	last Q	last /Q
x	1	last Q	last /Q

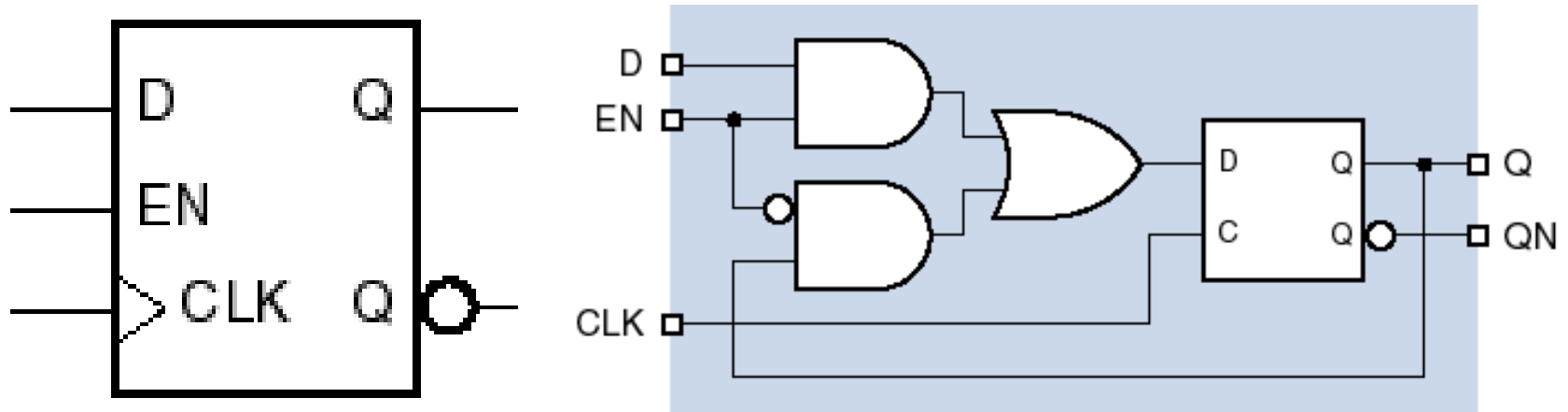




Flip Flop D con entradas asíncronas



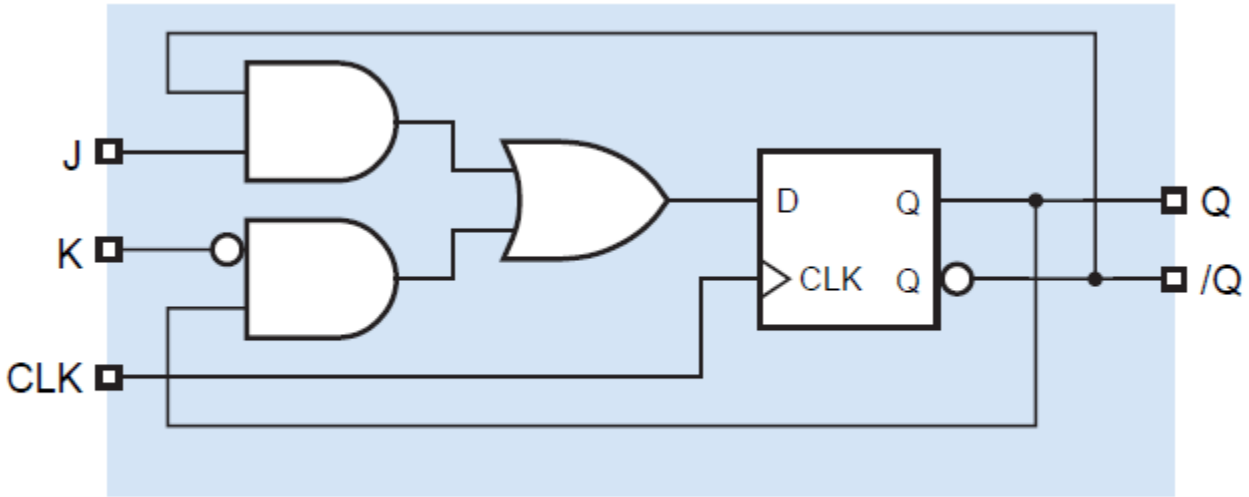
CLR	PR	CLK	Q
0	-	-	0
1	0	-	1
1	1		D
1	1	0, 1, 	Last Q

Flip Flop D con entradas habilitación

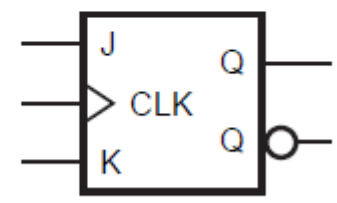


EN	CLK	Q
0	-	Last Q
1		D
1	0,1, 	Last Q

Flip Flop J-K

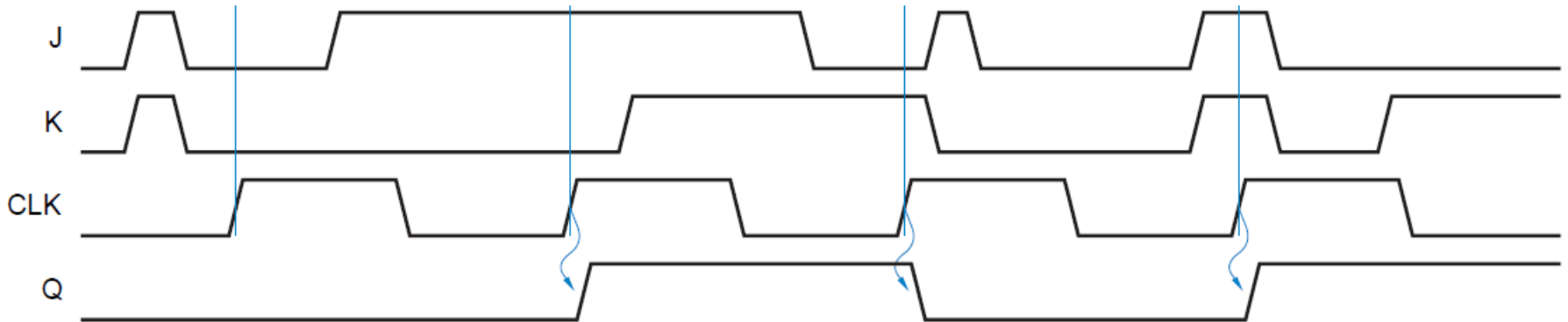
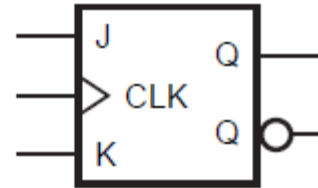


J	K	CLK	Q	/Q
x	x	0	last Q	last /Q
x	x	1	last Q	last /Q
0	0		last Q	last /Q
0	1		0	1
1	0		1	0
1	1		last /Q	last Q

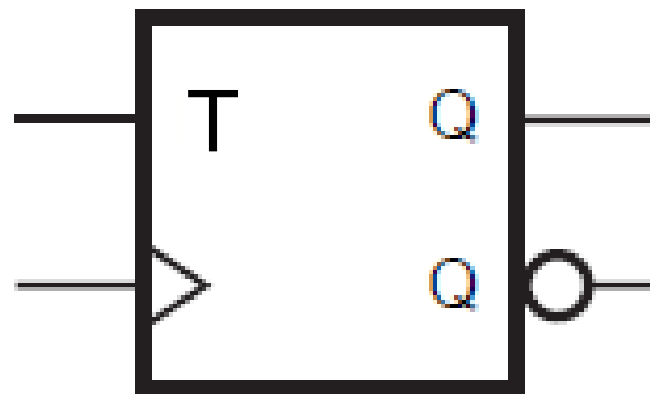
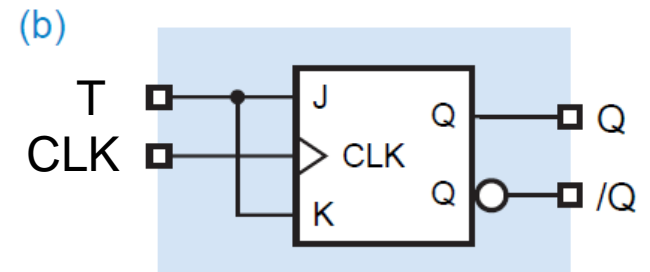
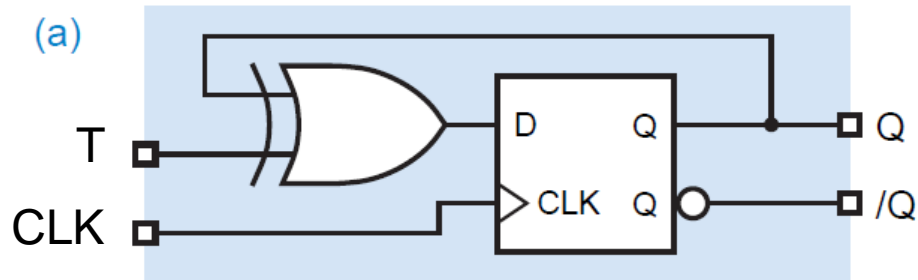


Flip Flop J-K

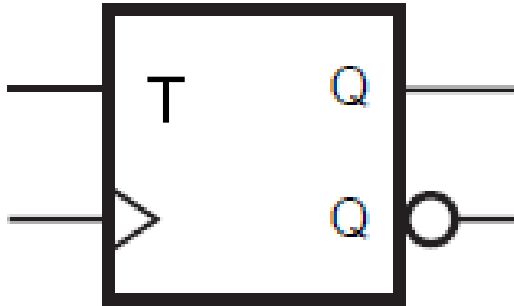
J	K	CLK	Q	/Q
x	x	0	last Q	last /Q
x	x	1	last Q	last /Q
0	0		last Q	last /Q
0	1		0	1
1	0		1	0
1	1		last /Q	last Q



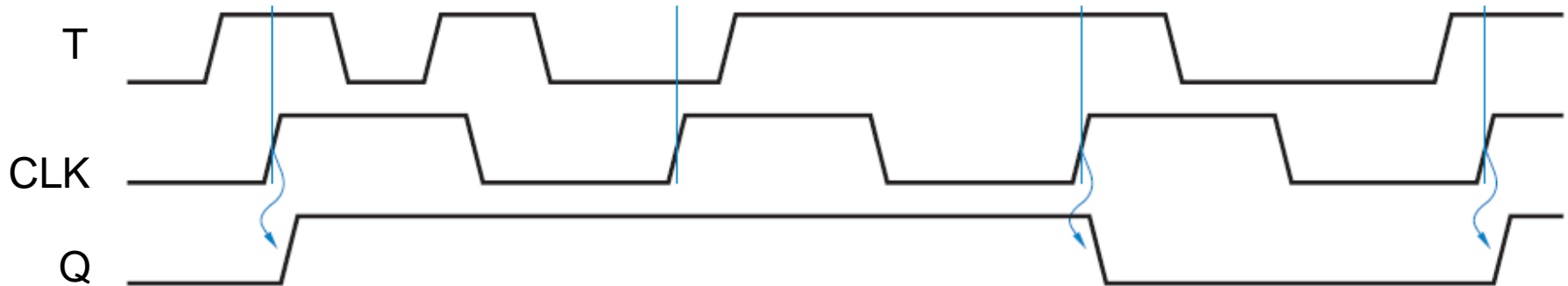
Flip Flop T



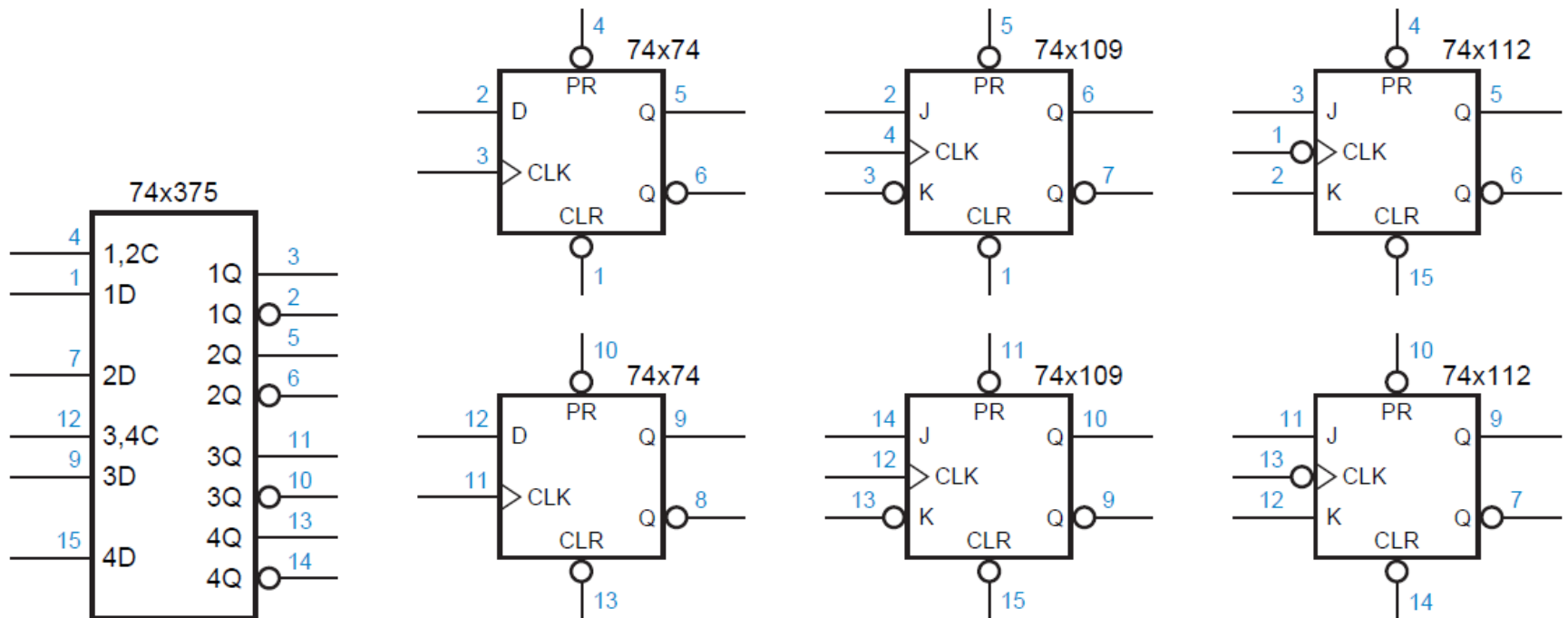
Flip Flop T



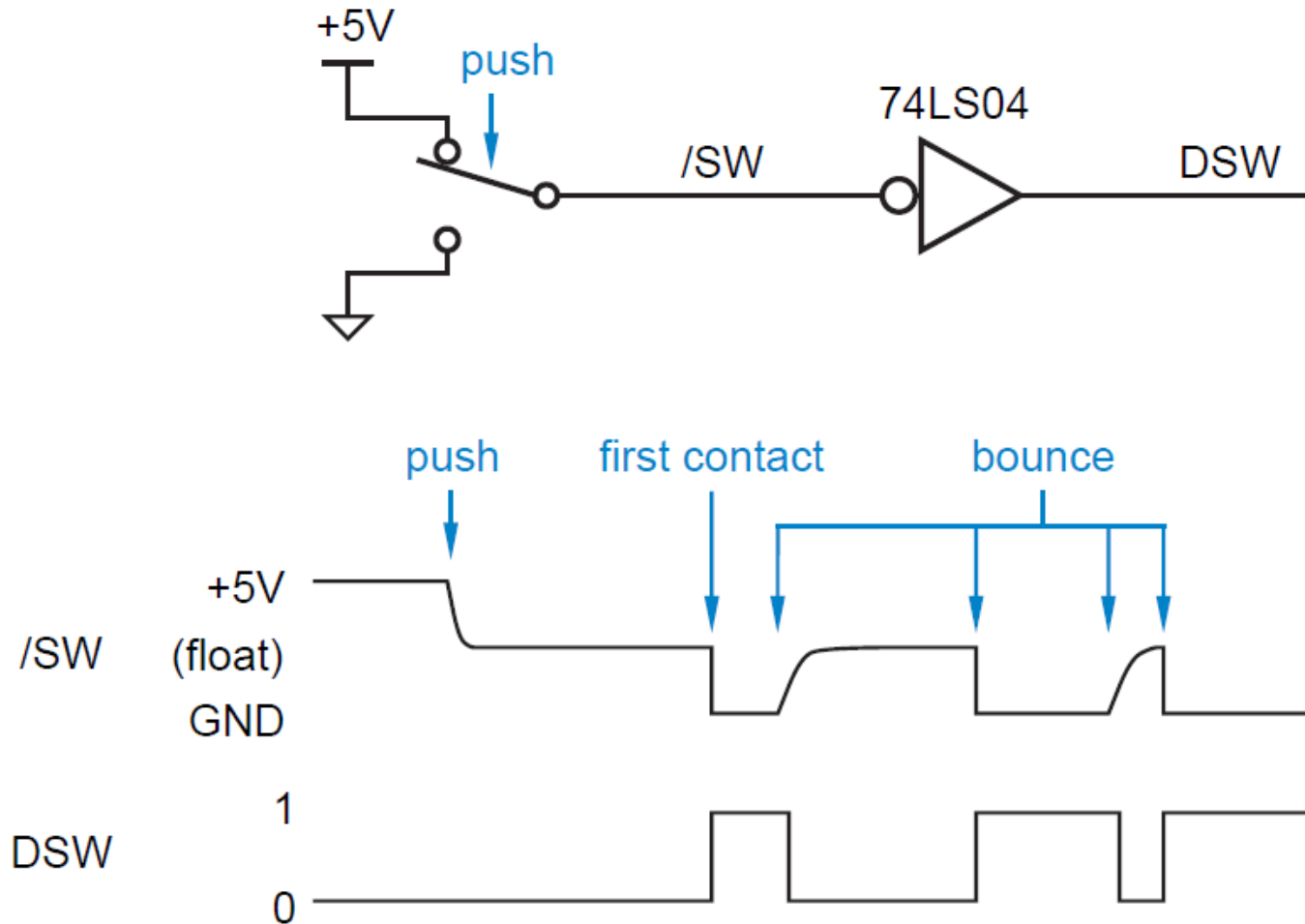
T	Q
0	Last Q
1	Last /Q



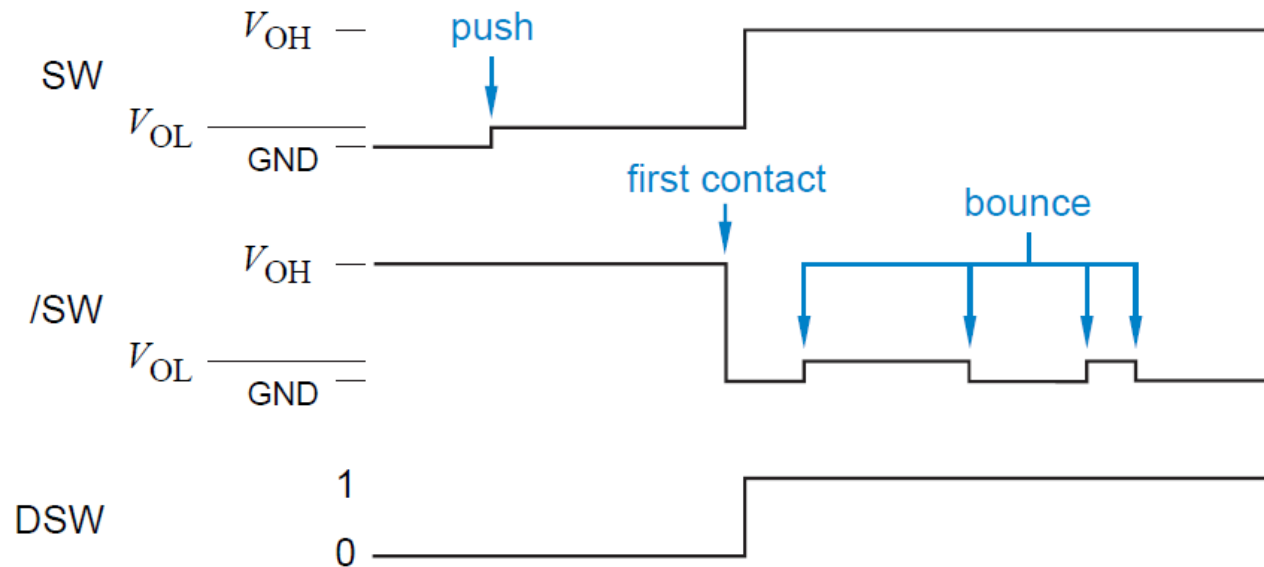
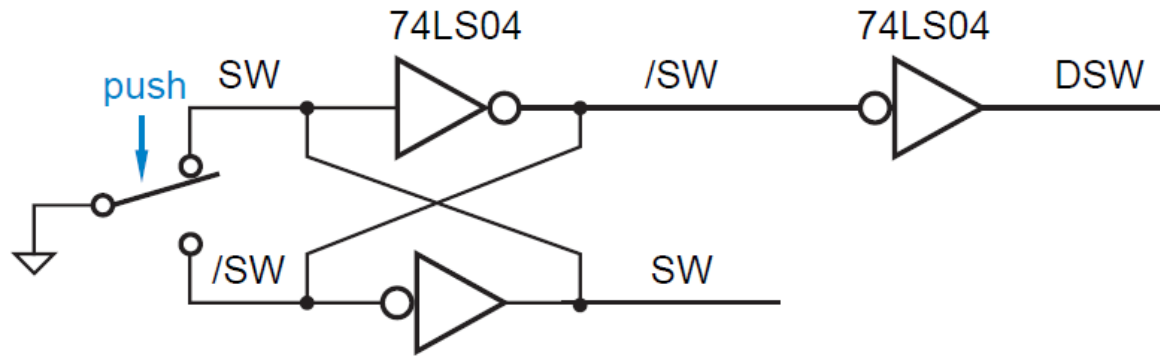
Latch y Flip Flop Comerciales



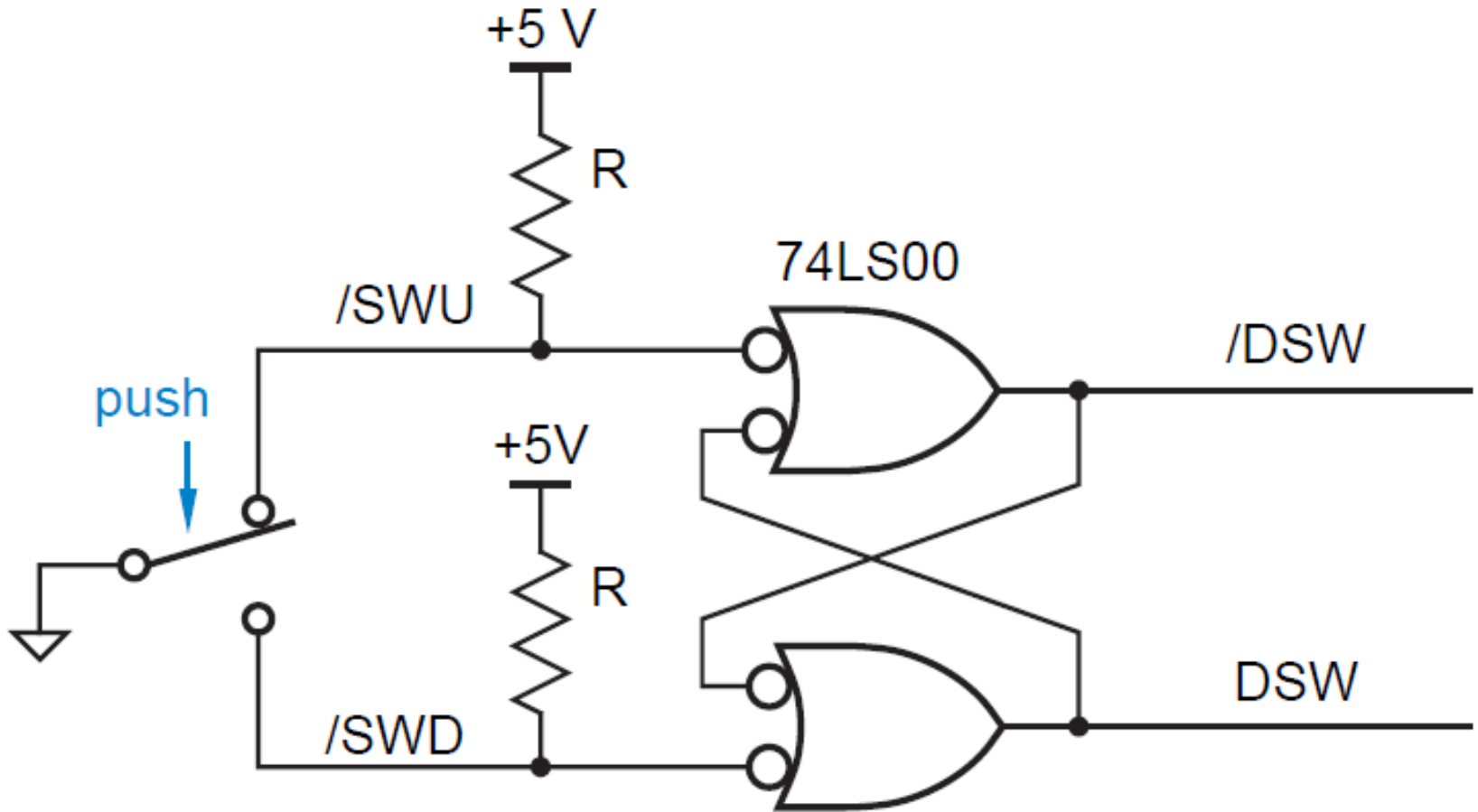
Rebote



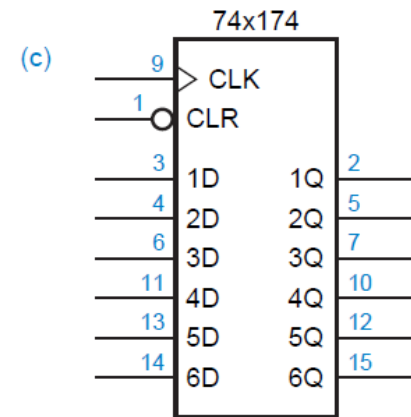
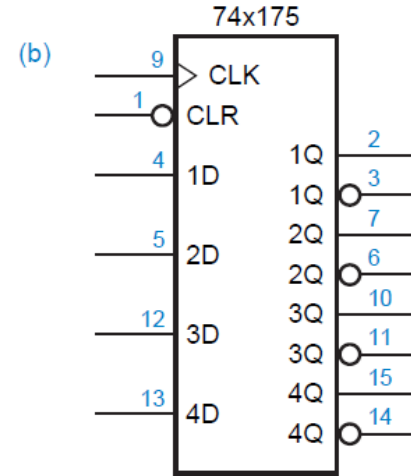
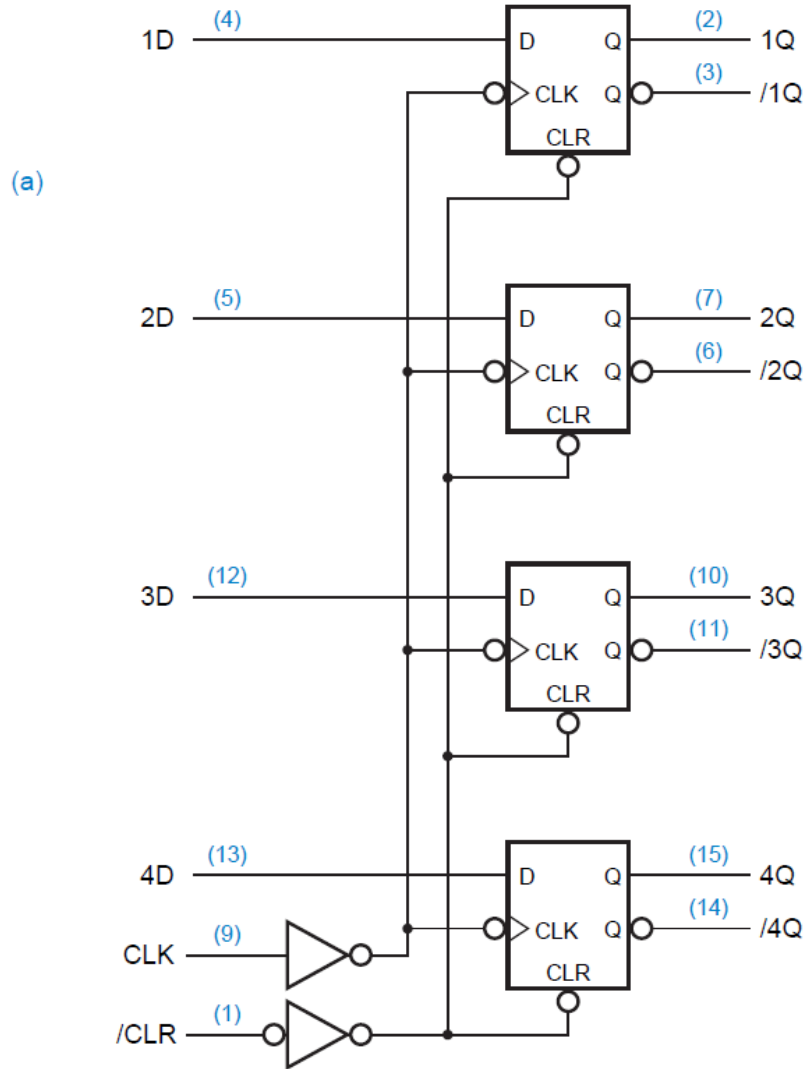
Rebote



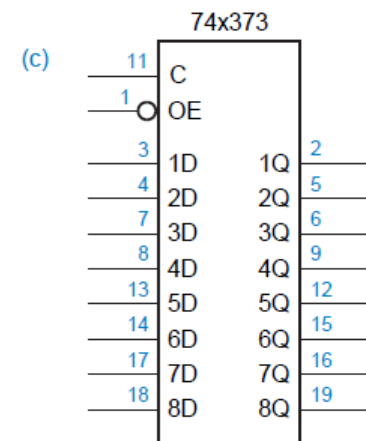
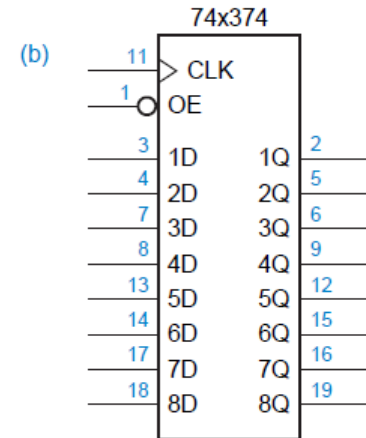
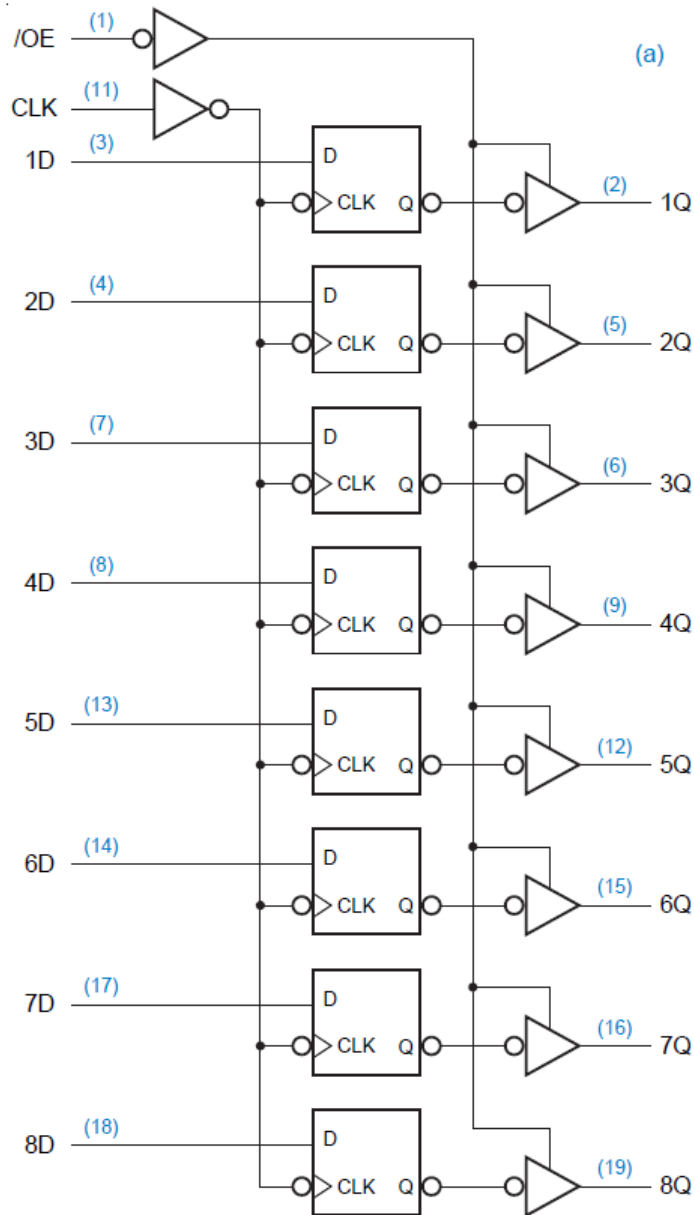
Rebote



Registros



Registros



Registros

