

ISA-RP55.1-1975 (R 1983)

Approved October 30, 1983

Recommended Practice

Hardware Testing of Digital Process Computers



ISA-RP55.1 — Hardware Testing of Digital Process Computers

ISBN 0-87664-392-6

Copyright ©1986 by the Instrument Society of America. All rights reserved. Printed in the United States of America. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means (electronic, mechanical, photocopying, recording, or otherwise), without the prior written permission of the publisher.

ISA
67 Alexander Drive
P.O. Box 12277
Research Triangle Park, North Carolina 27709

Preface

This Foreword, all footnotes and all Appendices are included for informational purposes and are not part of Standard ISA-RP55.1.

This Recommended Practice has been prepared as a part of the service of ISA toward a goal of uniformity in the field of instrumentation. To be of real value this document should not be static but should be subjected to periodic review. Toward this end the Society welcomes all comments and criticisms and asks that they be addressed to the Standards and Practices Board Secretary, ISA, 67 Alexander Drive, P.O. Box 12277, Research Triangle Park, North Carolina 27709. Telephone (919) 549-8411, e-mail: standards@isa.org.

During the 22nd Annual ISA Conference and Exhibit (Chicago, September, 1967) a workshop consisting of users experienced in digital process control convened under the auspices of the ISA Chemical and Petroleum Industries Division. The product of the workshop was a document titled "Consensus of Process Computers Users Workshop — Factory Hardware Witness Test Guidelines for Digital Process Computers." (References to the factory and witnessing were subsequently eliminated considering that the tests could be alternatively performed at the user's site and that documentation or other forms of compliance may be agreed upon.) The document was then mailed to digital process computer vendors, soliciting their comments.

Some of the underlying causes and needs that led to writing of that document were explained in a talk by Mr. Kirwin Whitman (workshop secretary) at the 9th National ISA Chemical & Petroleum Instrumentation Symposium (Wilmington, Delaware, April, 1968). This talk was subsequently published in the June, 1968, issue of *INSTRUMENTATION TECHNOLOGY*, and considerable industry response resulted. Therefore, a second workshop was held at the 23rd Annual ISA Conference and Exhibit (New York City, October, 1968) and included both users and vendors. The workshop resulted in consensus between users and vendors that a digital process computer hardware test standard was needed and what the scope and objective of the standard should be. A working committee composed of both users and vendors was formed to write the desired standard. The National Committee began meeting bimonthly starting in December, 1968; and six subcommittees (later increased to eleven) met in alternate months. In January, 1969, the ISA Standards and Practices Department gave official sanction to the committee, designating it as SP-55, Hardware Testing of Digital Process Computers.

The purpose has been to create a standard to serve as a guide for technical personnel whose duties include specifying, testing or demonstrating hardware performance of digital process computers. Basing engineering and hardware specifications, technical advertising and reference literature on this standard (or by referencing portions thereof, as applicable) will provide a uniform interpretation of the digital process computer's performance capabilities and the methods used for evaluating and documenting proof of performance. Adhering to the terminology, definitions and test recommendations developed will result in clearer specifications which should further the understanding between vendors and users.

The ISA Standards and Practices Department is aware of the growing need for attention to the metric system of units in general, and the International System of Units (SI) in particular, in the preparation of instrumentation standards. The Department is further aware of the benefits to users of ISA Standards in the USA of incorporating suitable references to the SI (and the metric system) in their business and professional dealings with other countries. Toward this end this Department will endeavor to introduce SI and SI-acceptable metric units as optional alternatives to English units in all new and revised standards to the greatest extent possible. *The Metric*

Practice Guide, which has been published by the American Society for Testing and Materials as ASTM E380-70, and future revisions, will be the reference guide for definitions, symbols, abbreviations and conversion factors.

The ISA Standards Committee on Hardware Testing of Digital Process Computers, SP55, operates within the ISA Standards and Practices Department, L. N. Combs, Vice-President. The persons listed below served as members of this Committee:

NAME	COMPANY
K. A. Whitman, Chairman	Allied Chemical Corporation
R. I. Baldwin	Sybron Corporation
J. Budelman	Electronic Associates, Inc.
R. F. Carroll	B. F. Goodrich Chemical Company
N. L. Conger	Continental Oil Company
G. G. Corwell-Kulesza	Motorola, Inc.
M. Fischer	Shell Oil Company
W. A. Fromme	Union Carbide Corporation
J. A. Glesias	Honeywell, Inc.
G. L. Joeckel, Jr.	General Electric Company
E. N. Pennington	Applied Automation Inc.
R. N. Pond	IBM Corporation
D. E. Sharp	United Engineering
R. A. Shaw	IBM Corporation
A. W. Sibol	E. I. du Pont de Nemours & Co., Inc.
R. L. Snyder	Control Data Corporation
M. G. Togneri	Fluor Corporation, Ltd.
Vernon Trevathon	Monsanto Company
A. Zikas	The Foxboro Company

The assistance of those who aided in the preparation of this Standard, by their critical review of the first draft, by offering suggestions toward its improvement, and in other ways, is gratefully acknowledged. In addition to SP55 committee members, the following have reviewed this Standard in its draft version and have thus served as a Board of Review. They have indicated their general concurrence with this Standard; however, it should be noted that, they have acted as individuals and their approval does not necessarily constitute approval by their company or facility.

NAME	COMPANY
J. J. Anderson	Watnation, Inc.
R. H. Appleby	E. I. du Pont de Nemours & Co., Inc.
J. S. Archer	Applied Automation, Inc.
C. L. Bare	Continental Oil Company
C. G. Barnkart	Bechtel Corporation
L. Basinski	Bechtel Corporation
F. M. Brent, Jr.	Dow Chemical Company
P. A. Brewster	Honeywell, Inc.
D. Bristol	Kaiser Aluminum & Chemical Corporation

G. L. Brown
B. W. Burdett
W. R. Cassel
P. J. Clelland
W. W. Cliffe
R. M. Cook
T. M. Couvillon
R. E. Dana
L. E. DeHeer
J. F. Derry
C. W. Doding
E. H. Dye
Keith O. Eaton
J. R. Egbert
T. L. Elmquist
M. J. Flanagan
H. R. Foster, Jr.
W. H. Geissler
G. J. Ginn
C. V. Godwin
K. W. Goff
P. M. Green
T. J. Harrison
N. Hatter, Jr.
D. R. Hibbs
G. Hohman
P. D. Hubbe
D. L. Hutchins
E. S. Ida
J. L. Inguanzo
T. J. Iwasaki
D. G. Jones
P. J. King
R. L. Knox
H. J. Kuschnerus
L. R. Leth
J. G. Lewis
Roy E. Lieber
B. T. Livingston
A. C. Lumb
A. C. McDonald
R. L. McIntyre
G. McLachlan
G. A. McNeill
F. C. Mears

Continental Oil Company
Kennectoo Computer Center
Delmarva Power & Light Company
Philadelphia Electric Company
Atomic Energy of Canada, Ltd.
Hewlett-Packard
IBM Corporation
Beloit Projects Inc.
E. I. du Pont de Nemours & Co., Inc.
Goodyear Tire & Rubber Company
C. F. Braun & Company
Ontario Hydro
Systems Engineering Labs.
EMR Computer
3M Corporation
Brown & Caldwell
Union Carbide Corporation
San Antonio Public Service Board
Sun Oil Company
Great Northern Paper Company
Leeds & Northrup Company
Bailey Meter Company
IBM Corporation
E. I. du Pont de Nemours & Co., Inc.
Inland Steel Company
EMR Computer
Great Northern Paper Company
Procter & Gamble
E. I. du Pont de Nemours & Co., Inc.
IBM Corporation
Sun Oil Company
A. D. Palmer Associates
B. P. Chemicals (UK) Ltd.
Control Data Corporation
Ford Motor Company
IBM Corporation
Consumers Power Company
Esso Research & Eng. Company
Houston Lighting & Power
Procter & Gamble
Imperial Oil Enterprises Ltd.
Detroit Edison Company
Scott Paper Company
Monsanto Company
Mobil Research & Development

C. W. Moexring
W. E. Moorman
V. S. Morello
A. V. Morisi
L. M. Mosely
K. A. Muranka
G. R. Nieman
J. A. Nyquist
J. F. Oakley
D. M. Ostfeld
K. M. Padegal
J. B. Palmer
M. R. Palmer
W. D. Perry
E. D. Pettler
H. G. Pinder
F. D. Plociennik
R. N. Pond
S. Rosenthal
R. A. Shaw
Thomas J. Shuff
I. I. Siegel
W. G. Simmons
R. Skrokov
D. L. Smith
W. W. Spencer
J. L. Stanley
J. H. Stubban
S. J. Suarez
D. R. Swann
T. H. Sweere
Walter Tetschern
G. A. R. Trollope
W. A. Van Valkenburgh, Jr.
W. B. Voss
Dan Wheelchel, Jr.
J. Wildberger
D. E. Williams
J. D. Wise
P. J. Womeldorff
D. W. Young
A. M. Yuile
D. W. Zobrist

Bechtel Corporation
Continental Oil Company
Dow Chemical Company
Boston Edison Company
Teledyne Geotech
Lockheed Electronics Company
Monsanto Company
Detroit Edison Company
EMR Computer
Tenneco Inc.
Bechtel Corporation
Applied Automation
Houston Lighting & Power
Weyerhouser

Taylor Instrument
Robertshaw Controls Company
IBM Corporation
Menasha Paperboard
IBM Corporation
Monsanto Company
Ebasco Services, Inc.
U. S. Steel
Union Carbide Corporation
Phillips Petroleum
General Electric
Union Carbide Corporation
Crown Zellerbach
Springfield Water Light & Power Co.
Commonwealth Edison
Varian Data Machines
EAI
Hooker
IBM Corporation
Hughes Aircraft Company
Cities Service Oil Company
Canadian General Electric
American Oil Company
Union Carbide Corporation
Illinois Power Oil
Interdata Inc.
Combustion Engineering
Alcoa

This Recommended Practice was approved by the ISA Standards and Practices Board in June 1971:

NAME

COMPANY

L. N. Combs, Vice-President

E. I. du Pont de Nemours & Co., Inc.

P. Bliss

Pratt & Whitney Aircraft Company

E. J. Byrne

Brown and Root Company

W. Carmack

Fisher Controls Company

R. E. Clarridge

IBM Corporation

G. G. Gallagher

The Fluor Corporation, Ltd.

R. L. Galley

U.N.O. Research Inst. for Instrument Design

E. J. Herbster

Mobil Oil Company

E. C. Magison

Honeywell, Inc.

J. R. Mahoney

IBM Corporation

F. L. Maltby

Drexelbrook Engineering Company

A. P. McCauley

The Glidden Company

W. B. Miller

Moore Products Company

D. Muster

University of Huston

H. N. Norton

Jet Propulsion Laboratory

G. Platt

Bechtel Corporation

C. E. Ryker

Cummins Engine Company

Contents

1 Scope	11
2 Factors to be considered	11
2.1 Use of the standard	11
2.2 Methods of compliance	12
2.3 Sequence, duration, and location of tests	12
2.4 Acceptance criteria for tests	12
2.5 Quantity of hardware tested	12
2.6 Special functions	13
2.7 Test equipment	13
2.8 Cost of testing	13
3 Recommended test, central processing unit	13
3.1 Objectives	13
3.2 Equipment to be tested	13
3.3 Test procedures	14
4 Recommended tests, data processing input-output subsystems	18
4.1 Objectives	18
4.2 Equipment to be tested	19
4.3 Test procedures	19
5 Recommended tests, digital inputs and outputs	36
5.1 Objective	36
5.2 Equipment to be tested	36
5.3 Test procedures	37
6 Recommended tests, analog inputs	39
6.1 Objective	39
6.2 Equipment to be tested	40
6.3 Test procedures	40

7 Recommended tests, analog outputs	49
7.1 Objective	49
7.2 Equipment to be tested	50
7.3 Test procedures	50
8 Recommended tests, interacting system	56
8.1 Objective	56
8.2 Equipment to be tested	56
8.3 Test procedures	57
9 Recommended tests, environmental	59
9.1 Objective	59
9.2 Equipment to be tested	60
9.3 Testing procedures	60
10 Documentation	62
10.1 Definition	62
10.2 Types of documents	62
10.3 Extent of documentation	62
10.4 User-vendor agreement	62
11 Glossary	63
11.1 Sources of definitions	63
11.2 Definitions	63
Appendix A — Analog input subsystem accuracy	71
Appendix B — Interacting systems	81
Appendix C — Environment	83

1 Scope

This ISA Recommended Practice establishes a basis for evaluating functional hardware performance of digital process computers. A process computer is typically characterized by the capability to acquire real-time data from a process in analog or digital form. In addition, a process computer generally has the capability to provide analog and digital control signals to the process.

This Recommended Practice covers general recommendations applicable to all hardware performance testing, specific tests for pertinent subsystems and system parameters, and a brief glossary defining terms used in this Recommended Practice. It identifies the tests to be considered and, in most cases, provides recommended procedures. Detailed specifications are necessary to define system acceptance criteria. Such specifications shall be negotiated between the vendor and user before the system is contracted.

The tests may be performed at the vendor's factory, the user's site or other suitable location. Furthermore, alternate methods of compliance such as certification or documentation of tests may be considered in place of directly performing the tests. Only equipment provided by the computer system vendor is within the scope of the Recommended Practice. Generally, this includes that equipment from the input terminations to the output terminations of the computer system.

The scope of this Recommended Practice does not include computer software testing, although certain software is necessary to perform the hardware tests. The tests do not evaluate reliability or availability. Destructive testing shall not be performed unless specifically agreed to by the vendor and user. It is also not intended that the Recommended Practice encompass interconnected multi-computer systems. These systems involve unique complexities, primarily in their software and interconnecting hardware, which were not specifically considered in the preparation of this Recommended Practice.

2 Factors to be considered

2.1 Use of the standard

The main intent of this Recommended Practice is to develop a common basic medium of communication between vendor and user. This is why it consists of the framework for a basic nucleus of tests. It is not the intent of this document to establish specifications or to set specific acceptance criteria because of the many differences which exist both in vendor product design and in user requirements.

All details of testing a specific computer system shall be negotiated before the system is contracted. A vendor's response to the requirements of this standard should be evaluated very carefully. Computer technology and methods of testing vary greatly between vendors and are continually changing. It is not the intent to label these recommended tests as the "State of the Art" or to use the Recommended Practice to prejudice a vendor or product.

2.2 Methods of compliance

The intent of the Recommended Practice may be satisfied in several ways. This could range from testing the complete system at the factory or the installation site, testing individual subsystems, use of demonstration systems, or other alternates such as certification and performance guarantees.

There are many factors which should be considered when negotiating the methods of compliance. Examples are as follows:

- 1) User's experience with the vendor's product
- 2) Vendor's normal testing methods and documentation
- 3) Past performance of vendor's equipment
- 4) Vendor's experience in the specific equipment design
- 5) Costs associated with each method of compliance

Witness testing may be specified as a means of compliance. This usually means the performance of tests in the presence of the user. This approach may not conform to the vendor's normal procedures and in most cases will result in some duplications of testing. This duplication, as well as the factors cited above, should be considered when negotiating compliance to this standard.

2.3 Sequence, duration, and location of tests

Vendors generally establish normal testing patterns which define sequence, duration, and location of tests. Obviously, these patterns vary from vendor to vendor. Careful consideration must be given to all deviations from these normal patterns of testing since deviations may increase or decrease the effectiveness of the testing and could involve extra costs.

2.4 Acceptance criteria for tests

Each test should have acceptance criteria based on conformance to the specifications referenced in the systems contract.

It is important to know which specifications apply to particular hardware testing configurations. Subsystem specifications often apply to individual devices or assemblies and may not be measurable or applicable at the system level. For the purposes of this Recommended Practice, the system specifications determining out-of-limit conditions shall be the subsystem specifications unless the vendor has separate system specifications.

Any special acceptance criteria or tests shall be negotiated and included in the system contract. The subsystem and system specifications must be altered to reflect all special acceptance criteria.

When a series of tests are performed, there should be agreement on how the failure of one test affects the others. Usually this can only be determined after the cause of the failure is known. Requirements for documentation of failure data should be established in accordance with 10, Documentation.

2.5 Quantity of hardware tested

These tests do not specify the quantity of similar hardware to be tested. For example, multiple peripheral devices and many process input and output channels are typically included in a system. The quantity and identity of such devices or channels to be tested shall be specified.

The manufacturing process may justify sample testing techniques at specific subsystem or system levels of assembly.

The testing of partially implemented, spare, and expansion functions should be considered. Specific tests and acceptance criteria for these functions should be defined.

2.6 Special functions

This Recommended Practice addresses tests which apply to typical digital process computers in today's marketplace. Where equipment configurations and functions differ from those outlined in this Recommended Practice, the test procedures shall be modified to reflect the individual equipment specifications.

2.7 Test equipment

Selection and certification of testing and measuring equipment is normally at the discretion of the vendor. Variations from this procedure should be negotiated when the system is contracted.

2.8 Cost of testing

Several areas throughout this Recommended Practice note that extra costs might be involved. As a general guide, extra costs may be incurred whenever a vendor is expected to deviate from his normal testing pattern.

Typical factors affecting the cost of testing are:

- 1) Number of separate test configurations required
- 2) Methods of compliance ([See 2.2](#))
- 3) Sequence, duration, and location of tests ([See 2.3](#))
- 4) Quantity of hardware tested ([See 2.5](#))
- 5) Special programming requirements
- 6) Special testing equipment
- 7) Effort required to prepare and perform tests
- 8) Documentation requirements ([See 10](#))

The additional testing costs may be justified through factors such as reduced installation costs, more timely installation, and early identification of application problems.

3 Recommended test, central processing unit

3.1 Objectives

The Central Processing Unit (CPU) tests are designed to demonstrate the capability of the CPU to perform all of its specified functions.

3.2 Equipment to be tested

Tests for the following CPU functions are included in this section:

- 1) Arithmetic and Control

- 2) Input-Output (I/O)
- 3) I/O Direct Storage Access
- 4) Hardware Interrupt
- 5) Hardware Timer
- 6) Main Storage

In cases where the CPU configuration differs from that described in this Recommended Practice, the test procedure shall be modified accordingly. Depending upon the storage capacity of the CPU subsystem, additional main storage hardware may be housed in a separate enclosure. For the purpose of the CPU test, all main storage is considered to be an integral part of the CPU subsystem.

Bulk storage, often considered as an extension of main storage for the storage of programs and data, may conveniently be tested concurrently with the CPU tests. Similarly, testing of consoles and certain other I/O devices are closely related to CPU functions. Test procedures for bulk storage and these I/O devices are described in 4, Data Processing Input-Output Subsystems.

3.3 Test procedures

Each of the following functions shall be tested individually and subsequently in combination as permitted by CPU configuration.

3.3.1 Arithmetic and control

All instructions, with all modes and options, shall be tested for operation in accordance with their specifications. Testing should be performed in a logical sequence, such as starting out with the basic load, store and transfer operations; progressing through the arithmetic, branch, and shift operations; logical, control operations, etc. I/O related operations such as direct storage access and interrupt tests are described in 3.3.3, I/O Direct Storage Access Channel, and 3.3.4, Hardware Interrupts.

3.3.1.1 Instruction load

A basic subset of instructions may be loaded through the computer control console or through any other conveniently available input medium. If the CPU has single cycle available, the basic subset of instructions can be executed in single cycle and the appropriate registers examined for correct results. If these instructions are entered through the control console, the switches and associated indicators (if any) should be examined for proper operation. Typical instruction complement may include:

- 1) Transfer Instructions
 - a) Load-Store Accumulator
 - b) Load-Store Index Register
 - c) Register-to-Register Transfer
 - d) Storage-to-Storage Transfer
- 2) Arithmetic
 - a) Add
 - b) Subtract
 - c) Multiply

- d) Divide
 - e) Arithmetic and Logical Shifts
- 3) Logical
 - a) OR (Logical Sum)
 - b) And (Logical Product)
 - c) Compare
 - d) Exclusive OR (Logical Subtract)
- 4) Control
 - a) Set Sign of Accumulator Positive-Negative
 - b) No Operation
 - c) Pause or Halt
 - d) Jump
 - e) Skip

3.3.1.2 Instruction execution

For testing efficiency, after the few basic instructions are tested by entering them through the control console keyboard or console switches, all other instructions can be checked by executing a program which manipulates all the instructions. The execution times of the instructions may be verified during this test. The program should be written so as to indicate the area of failure. For example, the program may automatically restart after completing a pass if no errors occur, or stop on an error condition. If an error is encountered, the area which failed should be identifiable from the stop address, program counter contents, or similar indication.

3.3.2 Input-Output (I/O) adapter(s)

3.3.2.1 Device address

A typical I/O requirement for the computer is to sense when devices are ready for transfer, to transmit control pulses to the peripheral devices, and to transfer data. The I/O channels generally operate on a party-line basis so that many devices may be connected to one channel. The peripherals are assigned device addresses which allow the computer to identify them. Each peripheral device address shall be generated and the test shall verify that only the addressed device responds.

3.3.2.2 BYTE manipulation

If hardware data packing or unpacking (byte assembly) capability is provided in the CPU or I/O devices, it should be tested by transferring data and verifying that the CPU or I/O device assembles or disassembles them correctly.

3.3.2.3 Device ready

In subsystems where data are transferred only when the device is ready, this operation shall be verified.

3.3.2.4 Error checks

Simulation of an error condition shall result in an interrupt or other action as specified in the subsystem specifications. Status or error functions of all devices should be checked using software where possible. If the subsystem has a status register that indicates the status or error condition of a device on the I/O channel, the register contents shall be examined for the proper indication. Status or error functions on a magnetic tape transport, for example, may indicate that the tape is being rewound or that a read error has occurred.

3.3.3 I/O Direct Storage Access Channel (DSAC)

This test verifies the complex of data paths, registers and controls which allow high speed I/O devices, such as magnetic tapes, drums, or disk files, to transmit data to and from main storage on a cycle-stealing basis.

3.3.3.1 Typical functions of the DSAC

Programmed subroutines shall test the following typical functions of the DSAC:

- 1) Initiation of DSAC operation by the specified I/O instructions
- 2) Independent I/O data transfer to and from the DSAC concurrent with mainline program operation. Multi-ported storage systems should be tested with all ports operating simultaneously.
- 3) Delay of the mainline program while DSAC data are transferred to and from main storage.

3.3.3.2 DSAC termination

Hardware termination methods may include transfer until the word count is zero (with or without a subsequent hardware interrupt), or transfer until a higher priority hardware interrupt is encountered. These and any other hardware DSAC termination methods should be tested to verify proper operation.

3.3.4 Hardware interrupts

If a hardware interrupt function is provided, all levels of interrupt are tested for proper sequencing and handling of hardware priorities. This can be accomplished using hardware or software simulation that sequentially causes each of the interrupt conditions to occur.

3.3.4.1 Interrupt acknowledge

A test shall be performed to verify that both internal and external hardware interrupts are properly acknowledged. By using software or hardware simulation, all interrupts shall be singly activated and the status of the system shall be verified to determine that proper acknowledgement occurs. If hardware functions are provided which automatically store or otherwise save the contents of registers, indicators, etc, in the correct operation of this function shall be verified.

3.3.4.2 Interrupt enable-disable

The master interrupt enable-disable (mask-unmask) controls and the enabling and disabling of individual interrupts (if provided) shall be tested. Through hardware or software simulation of interrupts on all available levels, it should be verified that hardware interrupts are acknowledged if and only if the proper combination of master and individual enable-disable conditions exist. If console or other indicators are provided to indicate the status of the interrupt structure, their proper operation shall be verified.

3.3.4.3 Multi-level interrupts

In typical hardware multi-level (priority) interrupt structures, the occurrence of an interrupt on a level higher than that currently being processed by the program results in a hardware initiated transfer to a storage location predefined by either hardware or software. In addition, the hardware initiated action may temporarily disable the interrupt structure and may provide automatic storage or other means of saving the contents of registers and indicators. When provided, these features shall be verified by an appropriate test. Using hardware or software simulation, interrupts may be simultaneously generated on various interrupt levels and the system status examined to verify that the interrupts were properly acknowledged. If automatic hardware disabling is provided, this may be tested by causing a series of interrupts such that a higher level interrupt occurs while the interrupt structure has been disabled by the hardware. Such an interrupt should not be acknowledged until the end of the disabling interval.

3.3.4.4 Power failure interrupt

In systems providing this feature, an interrupt is generated prior to the total failure of the primary power source. As a result of the interrupt, certain hardware initiated actions are performed to insure an orderly shutdown of the computer. During this shutdown procedure, automatic hardware or programmed subroutines may be used to save the contents of certain registers and system indicators. The purpose of this test is to verify that the specified hardware actions are accomplished prior to complete shutdown of the system. A power failure shall be simulated and the appropriate system parameters shall be observed to insure that the specified hardware actions have occurred. If a hardware save feature is provided, the saved data shall be verified after power is reapplied to insure that they have not been altered.

3.3.4.5 Auto-restart interrupt

If provided in the system, this feature provides for automatically restarting the CPU after a power failure. Although many of the actions required for auto-restart are software functions, certain hardware actions are required. A power failure shall be simulated and during the restart action the hardware functions shall be verified for proper operation.

3.3.4.6 Miscellaneous interrupt features

Other hardware interrupts or task control features shall be tested to verify proper operation.

3.3.5 Hardware timers

3.3.5.1 Interval timers

Hardware interval timers shall be checked to insure that they start and stop properly under program control. A specified number of time intervals shall be tested to verify timing accuracy. If the timer has hardware interrupt capability, a test shall be performed to check that the timer interrupts at the proper time. If provision is made for an external time base, an appropriate signal generator shall be connected to the timer input and the timer tested for proper operation.

3.3.5.2 Watchdog timer

If a watchdog timer is provided in the CPU, a test shall be performed to verify the activation of the alarm and reset functions. Under program control, a specified I/O instruction is executed to insure that the watchdog timer resets. Operation of the alarm function is tested by blocking or bypassing the I/O instruction and verifying that all specified timer functions operate properly.

3.3.5.3 Real-time timer

If a hardware real-time timer which is not software dependent is included in the CPU, a test shall be performed to compare the timer against a calibrated time base.

3.3.6 Main storage

3.3.6.1 Addressing

Addressing shall be tested by loading a specified number of main storage locations with their own addresses. Read out these storage locations and compare to verify correct addressing.

3.3.6.2 Worst case pattern test

This test, sometimes referred to as the Delta Noise or Checkerboard Test, shall be performed by storing into main storage the worst case data pattern for the particular storage design and addressing scheme used by the vendor. Such a test normally loads a major segment of main storage with this pattern so as to produce the worst possible signal-to-noise ratio. The data are written, read back, complemented, and written again on repeated storage cycles. The test should be executable for more than one segment of main storage. When this option is available, the entire main storage can be tested for stability.

3.3.6.3 Circuit load test

This test is designed to identify circuit loading and adjacent bit noise problems. The main storage shall be tested using a "floating one" and a "floating zero" pattern. The "floating one" test is performed by loading one word with all zeros except for a one in the most significant bit position. The word is read, compared to its expected bit pattern and, if correct, is shifted one position to the right and restored in the next higher storage location. The procedure is repeated until all storage locations have been tested. The "floating zero" test is identical except that a word containing only a single zero is used.

3.3.6.4 Storage protect

This test is designed to verify that protected areas of main storage are not violated when hardware storage protection is provided. A preselected area of main storage shall be loaded with a known data pattern and storage protection of the selected area activated by means of the appropriate mechanism (bit, area code, etc.). An attempt to violate the protected area shall result in a violation signal, indicator, or interrupt. It shall be verified that the protected data were not modified. A test shall be performed to verify that storage protection can be deactivated so that the selected area is restored to the unprotected status. All areas capable of being hardware protected shall be tested in a similar manner. If the hardware protection can be program controlled, the control instructions shall be tested to verify proper operation. All other hardware protect features shall be tested.

4 Recommended tests, data processing input-output subsystems

4.1 Objectives

Data Processing Input-Output (DP I/O) Subsystems tests are directed at insuring proper function of I/O subsystems which are part of typical digital process computer systems. These tests are designed to verify functions at the subsystem level only. They do not cover interacting systems testing which is defined in 8 Interacting System.

For the purposes of this standard, the elements of the Data Processing Input-Output Subsystem include:

- 1) The attachment circuitry, which is housed in the CPU and which furnishes logic controls along with data links to the I/O bus.
- 2) The controller, which provides the buffer between the I/O bus and the I/O device itself. The controller may provide a variety of functions to minimize the requirement for a direct interaction between the I/O device and the main CPU data paths. Typical functions provided in the controller include control of cycle-stealing operations, error checking, and device address coding. The controller is not a necessary part of the subsystem: many subsystem designs specify direct connection of the device to the CPU.
- 3) The I/O devices, which provide bulk storage, card or paper tape processing, printed output, terminal communication, and other data processing functions.

4.2 Equipment to be tested

In cases where the I/O equipment configurations differ from those described in this standard, the test procedure should be modified or additional tests defined to conform to the equipment specifications. Tests for the following I/O subsystems are included in this section:

- 1) Card Readers and Punches
- 2) Paper Tape Readers and Punches
- 3) Disk Storage Devices
- 4) Drum Storage Devices
- 5) Magnetic Tape Devices
- 6) Typers and Line Printers
- 7) Video Display Stations
- 8) Data Collection Terminals
- 9) Data Modems
- 10) Keyboards and Consoles

4.3 Test procedures

4.3.1 Card readers and punches

The device to be tested may be a reader only, a punch only, or a combination reader-punch unit. Hollerith or various binary codes may be used as specified for the particular I/O subsystem.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Punch and Read Operations
- 4) Card Transport

4.3.1.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Failure to feed from input hopper
- 2) Empty input hopper
- 3) Punch die not seated
- 4) Card jam detection
- 5) Full stacker condition
- 6) Door and cover interlocks
- 7) Full chad box
- 8) Chad box not installed
- 9) Crank interlock
- 10) Last card feed operation

4.3.1.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators to be tested include:

- 1) Keys and Switches
 - a) Start Key
 - b) Stop Key
 - c) Runout Key
 - d) Load Key
 - e) Single-Cycle Switch
 - f) Reset Key
 - g) Power-On Switch
 - h) Duplication Key
- 2) Indicators
 - a) Ready or Go Indicator
 - b) Halt or Not-Ready Indicator
 - c) Power-On Indicator
 - d) Error Indicators

4.3.1.3 Punch and read operations

Read and punch speed shall be tested in accordance with specifications (cards processed per minute in a continuous feed mode).

All alphanumeric or binary characters shall be tested in accordance with the character configurations defined in the specifications. Illegal characters shall cause the specified error indications. A typical pattern (alphanumeric) may include the following character configuration:

ABCD . . . Z0123 . . . 9@-\$+ . . .*ABCD. . .

Various character configurations (in a random mode, sequential mode, etc.) shall be used to test for multiple or missing reads and for multiple or missing punches. Typical patterns may include:

Card #1 - ABCD.....9@\$+

Card #2 - BCDE.....@\$+—

Card #3 - CDEF.....\$+—#

etc.

Card #1 - IQXHPWGOVFNVEMTDLSCK...

Card #2 - QXHPWFOVFNVEMTDLSCKI...

Card #3 - XHPWFOVFNVEMTDLSCKIQ...

Vertical and horizontal read registration shall be tested by verifying the ability to read prepunched cards whose punch holes are at the prescribed specification limits for this parameter.

The punched card output of the punch shall be tested with a card gage or similar device to verify proper vertical and horizontal registration of the punched holes. Consistency of registration shall also be examined.

4.3.1.4 Card transport

Cards shall be examined for marks, tears, and bends on faces or edges which may indicate improper card transport or mechanical interference. Corner cut cards with various corner cut configurations shall be used to verify proper card transport and feed.

If there are multiple stackers, stacker select operations shall be tested for all specified commands. Individual stackers may be selected as a function of error conditions, character coding, and other selection instructions identified in the specifications.

4.3.2 Paper tape readers and punches

Paper tape readers and punches may specify the use of 5-, 6-, 7-, or 8-channel tape. Depending upon the specifications, the device may be required to process tape made of oiled or non-oiled paper, of a metalized plastic material, or a combination of the above.

The tape may be either chad or chadless. Chad tape is defined as tape which has all holes completely punched out. If chadless tape is used, all chad shall be on the side of the tape away from the reading mechanism. The test method shall allow for configurations of feed mechanisms which are designed to handle strip feed, center-hole feed, or reel feed.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Punch and Read Operations
- 4) Paper Tape Transport

4.3.2.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified.

All specified indicators shall be activated. Typical interlock conditions include:

- 1) Empty supply reel or tape runout
- 2) Tape guide arms not seated
- 3) Tape tension detection
- 4) Door and cover interlocks
- 5) Full chad box
- 6) Chad box not installed

4.3.2.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators include:

- 1) Keys and Switches
 - a) Delete Key
 - b) Feed Key
 - c) Reset Key
 - d) Start Key
 - e) Stop Key
 - f) Reel or Strip-Select Switch
 - g) Single-Cycle Switch
 - h) Power-On Switch
- 2) Indicators
 - a) Ready or Go Indicator
 - b) Halt or Not-Ready Indicator
 - c) Power-On Indicator
 - d) Error Indicators

4.3.2.3 Punch and read operations

Punch and read speed shall be tested in accordance with specifications (characters read or punched per second in a continuous mode).

All alphanumeric or binary characters shall be tested in accordance with the character configurations identified in the specifications. Illegal characters shall cause the specified error indications. A typical test pattern (alphanumeric) may include the following character configurations:

ABCD . . . Z0123 . . . 9@-\$+ . . .*ABCD. . .

Various character configurations (in a random mode, sequential mode, etc.) shall be used to test for multiple or missing reads and for multiple or missing punches. Typical test patterns are described in 4.3.1.3, Punch and Read Operations.

The punched tape output shall be examined to verify proper longitudinal registration. A standard tape gage or similar device may be used.

The punched tape shall be tested to verify that all feed holes are punched as blank tape advances through the punch station, If so specified, duplicate feed hole punching shall not occur during a backspace or reverse operation.

4.3.2.4 Paper tape transport

Tapes shall be examined for marks, tears, elongated holes, and raised edges on feed and channel holes which may indicate improper tape transport or mechanical interference at the punch or read station. Tape dispensing and take-up functions shall also be tested using various amounts of tape on the tape reels.

Forward and reverse tape motion during punch and read operations shall be tested by verifying that a specified backspace/forward routine is initiated on command.

Various combinations of short and long tape motions shall be used to test for proper tape feed, tape registration, and read-punch functions.

4.3.3 Disk storage devices

These tests apply to single or multiple disk configurations which use fixed disks or customer-removable cartridges. The tests are also applicable to fixed head or moveable head devices. (A fixed head device has its heads permanently located over specified track locations. A moveable head device has its heads mounted on a moveable access mechanism which may be positioned opposite any track location on the disk surface.)

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Read and Write Operations
- 4) Seek or Access

4.3.3.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Cartridge or Disk-Pack Removal Interlock
- 2) Cover Interlock
- 3) Read or Write Circuit Protect
- 4) Over- or Under-Voltage Detection
- 5) Speed Detection
- 6) Head Load, Unload, or Position Interlock
- 7) Pressurization Interlock

4.3.3.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators include:

- 1) Keys and Switches
 - a) Head-Select Switch
 - b) Incremental Step Switch
 - c) Incremental Direction Switch
 - d) Head-Load Switch
 - e) Reset Key
 - f) Power-On Switch
 - g) Start Key
 - h) Stop Key
- 2) Indicators
 - a) Head-Select Indicator
 - b) Power-On Indicator
 - c) Ready Indicator
 - d) Drive-Number Indicator
 - e) Cartridge/Pack Status Indicator
 - f) Read/Write Protect Indicator
 - g) Error Indicator

4.3.3.3 Read and write operations

Data shall be transferred to and from the entire recording surface of the disk storage device to verify the operation of specified read and write functions. Cross-talk tests shall be performed to verify read and write functions on adjacent tracks. Various data patterns and record lengths shall be used to simulate worst-case bit patterns if so specified. Interchangeability of disk packs between disk storage devices shall also be verified. Typical functions to be tested in this type of device include:

- 1) Accessing to all track addresses in a serial access mode (including return to zero or home).
- 2) Random accessing to track addresses so that the access mechanism is required to make both long and short movements. Random accessing verifies such functions as:
 - a) Forward Fast
 - b) Forward Slow
 - c) Reverse Fast

- d) Reverse Slow
- e) Stop and Detent
- f) Access Time (Average and Maximum)

4.3.4 Drum storage devices

Drum storage devices may be configured with a magnetic drum unit which is vertically or horizontally mounted. The read/write heads are typically fixed at a specified track location over the drum surface.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Read and Write Operations

4.3.4.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Thermal Overload
- 2) Speed Detection
- 3) Pressurization Interlock
- 4) Over- or Under-Voltage Detection
- 5) Head Position Interlock
- 6) Read or Write Protect

4.3.4.2 Operational keys, switches, and indicators

The operation of all keys, switches, and interlocks shall be tested according to specification. Typical keys, switches, and indicators include:

- 1) Keys and Switches
 - a) Head-Select Switch
 - b) Power-On Switch
 - c) Head-Load Switch
- 2) Indicators
 - a) Head-Select Indicator
 - b) Power-On Indicator
 - c) Head-Load Indicator
 - d) Error Indicator

4.3.4.3 Read and write operations

Data shall be transferred to and from the entire recording surface of the drum storage device to verify the operation of specified read and write operations, including the write protect function.

Cross-talk tests shall be performed to verify read and write function on adjacent tracks. Various data patterns shall be used to simulate worst-case bit patterns if so specified. Typical functions tested during read and write operations include:

- 1) Proper head and address selection as a function of the unique address associated with the identifying bits or bytes.
- 2) End-of-record recognition using variable data lengths.
- 3) Data transfer rate in a continuous read mode.

4.3.5 Magnetic tape devices

The individual specifications for the magnetic tape device may permit the use of seven- or nine-track magnetic tape. The grades or types of tape may be specified in accordance with the tape bit densities and other characteristics of the device. The test method shall allow for configuration of magnetic tape devices which are designed to handle full reels, miniature reels, or cartridges of magnetic tape.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Read and Write Operations
- 4) Tape Transport

4.3.5.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Reel, Door, and Tape Mechanism Interlocks
- 2) Thermal Overload
- 3) Over- or Under-Voltage Detection
- 4) Tape or File Protect
- 5) Tape Tension Detection
- 6) Head-Unload or Load Failure

4.3.5.2 Operational keys, switches, and indicators

The operation of keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and interlocks include:

- 1) Keys and Switches
 - a) Start Key
 - b) Stop Key
 - c) Reset Key

- d) Tape-Load Key
 - e) Tape-Rewind Key
 - f) Reel-Release Switch
- 2) Indicators
 - a) End-of-Tape Indicator
 - b) Tape or File Protect Indicator
 - c) Select or Drive Number Indicator
 - d) Ready Indicator
 - e) Thermal or Voltage Failure Indicator
 - f) Error Indicator

4.3.5.3 Read and write operations

To verify proper function of the read or write operation, data shall be transferred to and from the magnetic tape device. Interchangeability of magnetic tapes between magnetic tape devices shall also be verified. Worst-case bit patterns and timings shall be used if so specified. Typical functions tested during the read and write operations include:

- 1) Horizontal Validity Check
- 2) Record Validity Check
- 3) Write Check
- 4) Load Point (Start Read or Write)
- 5) End-of-Tape
- 6) Data Block Recognition
- 7) Read Backwards
- 8) Backspace (no data transferred)
- 9) Erase Tape

4.3.5.4 Tape transport

The tape transport is activated when commands to read, write, read backward, rewind, or unload are received by the tape device while it is in a ready status. Short and long records shall be read and written to test for proper functions of drive clutches and tape positioning mechanisms. High and low speed rewind functions shall also be verified along with start-stop time if so specified.

4.3.6 Typers and line printers

This procedure defines the test requirements to verify proper function of the output printing devices. The output printer may be a teletypewriter, a typewriter, or a line printer.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators

- 3) Print Operations
- 4) Carriage and Forms Transport

4.3.6.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Cover Interlocks
- 2) Print-Protect Shield Not In Place
- 3) Forms Runout
- 4) Forms Jam
- 5) Platen Not Installed
- 6) Printer Not Ready

4.3.6.2 Operational keys, switches, indicators, and manual controls

All keys, switches, indicators, and manual controls shall be tested according to specifications. Typical keys, switches, indicators, and manual controls include:

- 1) Keys and Switches
 - a) Start Key
 - b) Stop Key
 - c) Forms-Runout Key
 - d) Space Key
 - e) Carriage-Restore Switch
 - f) Reset Key
 - g) Power-On Switch
 - h) Program Interrupt Key
- 2) Indicators
 - a) Ready or Go Indicator
 - b) Halt or Not-Ready Indicator
 - c) Power-On Indicator
 - d) Error Indicators
- 3) Manual Controls
 - a) Carriage Clutch
 - b) Forms Thickness Adjustment
 - c) Paper Release Lever

4.3.6.3 Print operations

Printer speed shall be tested in accordance with specifications (lines-per-minute or characters-per-second in a continuous print mode).

All alphanumeric or binary characters (in a random mode, sequential mode, etc.) shall be tested in accordance with the character configurations identified in the specifications. Worst-case test patterns shall be used if so specified. A typical test pattern may include the following character configuration:

ABCD . . . Z0123 . . . 9@-\$+ . . . *ABCD . . .

Various character configurations are to be tested as a function of the parallel or serial mode of the individual printer and as a function of the device specifications. Each line of print shall be checked to insure that the specified number characters are printed within the margins. Typical character configurations may include:

Line #1 - ABCD.....9@\$+

Line #2 - BCDE.....@\$+-

Line #3 - CDEF.....\$+-#

etc.

Line #1 - IQXHPWFOVFNEMTDLSCK...

Line #2 - QXHPWFOVFNEMTDLSCKI...

Line #3 - XHPWFOVFNEMTDLSCKIQ...

etc.

A printer output test shall be performed to verify that all specifications for print quality are met. Typical print quality specifications include:

- 1) Character Alignment
- 2) Spacing Between Adjacent Characters
- 3) Uniformity of Character Impressions
- 4) Multiple Copy Legibility

4.3.6.4 Carriage and forms transport

Forms shall be checked for marks, tears, bends, or burred edges which may indicate improper forms transport or mechanical interference. Pin feed platens shall be checked to insure that pins operate properly and that forms tension conforms to specifications.

Carriage spacing, skipping, and other specified functions shall be tested. Typical specified functions include:

- 1) Ribbon Color Control
- 2) Carriage Return
- 3) Tabulate
- 4) Space and Backspace
- 5) Double and Triple Space
- 6) Space Suppress

- 7) Skip-To Immediate
- 8) Skip-To Delayed
- 9) Line Feed
- 10) Overflow
- 11) Left Margin Registration

Line printers which use a punched tape or similar technique to control the length of a skip operation shall be tested by skipping to the location identified by the control technique established in the specifications.

4.3.7 Video display stations

The video display station may serve as a slave image projector or it may incorporate a controller as well as a keyboard entry or inquiry unit. A typical process control system may connect to an array of video display stations.

All specified functions shall be tested. Typical functions include:

- 1) Operational Keys, Switches, and Indicators
- 2) Image Characteristics

4.3.7.1 Operational keys, switches, and indicators

- 1) Alphanumeric Keys: As each key is operated, the specified character shall be displayed at the proper location. Keying speed and code accuracy shall be tested if so specified.
- 2) Space and Backspace Keys: Depression of the space key shall place a blank at the proper location. When the backspace key is activated, the initially displayed character shall be erased, if so specified.
- 3) Erase Display: Use of the erase display key shall result in complete erasure of the entire display if this function is specified.
- 4) Special Functions: The enter, shift, start, end-of-message, cursor, and other functions shall be tested if so specified.
- 5) Indicators and Switches: All indicators shall switch to the proper status as defined in the specifications. These indicators may include Ready, Enter, Halt, Error, Power-On. All switches shall be functionally tested according to specifications.

4.3.7.2 Image characteristics

All specified image characteristics shall be examined based on an all-character display pattern or other patterns as specified for individual parameters. An over-lay mask, a display measurement system, or other equivalent test aids shall be used in verifying specified image characteristics.

Typical image characteristics which shall be examined in accordance with specifications include:

- 1) Centering
- 2) Squareness
- 3) Size
- 4) Vertical Linearity

- 5) Horizontal Linearity
- 6) Distortion
- 7) Stability
- 8) Brightness
- 9) Contrast
- 10) Focus
- 11) Color
- 12) Image Retention

All accessible adjustments shall be checked to verify specified operation over the full range of control. Typical adjustments may include:

- 1) Brightness
- 2) Focus
- 3) Contrast
- 4) Horizontal Hold
- 5) Vertical Hold
- 6) Color

4.3.8 Data collection terminals

Data Collection Terminal subsystems may be connected to the CPU via a central control station which has communication to other satellite I/O stations. A two-wire cable system typically provides the coupling to the digital process computer and to the other satellite stations. I/O devices incorporated within the terminal subsystem may include readers, printers, digital time units, and manual entry devices. Reader or punch units may accept cards, badges, or cartridges depending on configuration.

All specified functions shall be tested. Typical functions include:

- 1) Interlocks
- 2) Operational Keys, Switches, and Indicators
- 3) Transmit and Receive Operations

4.3.8.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

- 1) Manual Entry Send
- 2) Card Reader Send
- 3) Badge Reader Send
- 4) Repeat or Resend Message
- 5) Digital Time Clock Interrupt

- 6) Input Edit Check
- 7) Printer Not-Ready
- 8) Satellite Power Failure
- 9) Cover Interlocks

4.3.8.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators include:

- 1) Keys and Switches
 - a) Clear or Restore Key
 - b) Manual Send Key
 - c) Mode-Select or Input-Output Device-Select Switch
 - d) Clock Reset or Digital Time Reset Key
 - e) Start or Stop Key
 - f) Manual Reset Key
 - g) Backup Mode Switch
 - h) Power-On Switch
- 2) Indicators
 - a) Badge, Card, or Manual Ready Indicator
 - b) Repeat or Resend Indicator
 - c) Busy or In-Process Indicator
 - d) Clock Failure Indicator
 - e) Standby Indicator
 - f) End-of-Forms Indicator
 - g) Power-On Indicator
 - h) Receive or Send Indicator

4.3.8.3 Transmit and receive operations

To verify proper function of the transmit or receive operation, data shall be transferred to and from the data terminal devices. Typical tests for the functional operation of transmit and receive include:

- 1) Input Edit Control
- 2) Record Validity Checking
- 3) Sequential Polling
- 4) End-of-Transmission
- 5) Record Length Checking

4.3.9 Data modems

Modems are designed for half-duplex or full-duplex operation. Depending on the equipment to which it is connected and the quality of the transmission line, the modem may operate at various specified transmission speeds and carrier frequencies. In all cases the recommended tests shall conform to the specifications for the modem under test.

When applicable, the interface connection between the modem and the digital equipment shall be in accordance with communications interface standard EIA RS232.B

It should be noted that modem equipment is frequently provided by a common carrier vendor rather than the computer vendor. In such a case, testing arrangements may be required with the common carrier vendor.

All specified functions shall be tested. Typical functions include:

- 1) Signal Conditioning
- 2) Equalization
- 3) Performance
- 4) Control and Interchange Circuits

4.3.9.1 Signal conditioning

The tests for signal conditioning for both the input and output interfaces, excluding controls, shall typically address the following parameters:

- 1) Voltage Amplitude (Mark and Space)
- 2) Impedance (Resistive and Capacitive)
- 3) Rise and Fall Times
- 4) Grounding (Frame and Signal)
- 5) Attenuation

4.3.9.2 Equalization

Compensation for line characteristics may be specified as either manual or automatic. In the manual case, the test shall demonstrate performance over the full range of line characteristics specified. Testing for automatic compensation shall, in addition to testing for line variation limits with specified error rate performance, include sufficient dynamic tests to verify compensation response times for step-function changes in line characteristics. Criteria for determining response time should be in terms of the time required to recover to specified error rate performance. Typical parameters to be checked include envelope delay, amplitude, and linearity.

4.3.9.3 Performance

Performance parameters to be measured typically include data rate and error rate for specified line characteristics and signal-to-noise ratio. Testing shall be conducted for each specified data rate of a multispeed unit. Measurement of error rate may require a modulator-demodulator pair connected by a link that permits line simulation.

A pseudo-random code pattern of specified length or other suitable patterns may be utilized in determining error performance. Demodulator tests should demonstrate acquisition time.

4.3.9.4 Control and interchange circuits

Functions and parameters to be tested typically include:

- 1) Manual or external control of data rate (as specified for synchronous and asynchronous modes)
- 2) Synchronizing signals which are internally generated.
- 3) Response to control signals such as Request-to-Send, Clear-to-Send, Interlock, Transmitted Data, Received Data, and Received Signal Detection.
- 4) Applicable control signal, voltage levels, frequency, waveshape, and noise rejection levels.
- 5) Amplitude range and the time relationship between critical control signals. Modem-generated control signals to external interface equipment shall be measured for amplitude, timing, and frequency when terminated with the specified load.

4.3.10 Keyboards and consoles

The procedure describes the test requirements to verify proper functional operation of keyboards and consoles. In typical applications, keyboards and consoles are housed adjacent to or within a CPU frame. Keyboard and consoles are also housed within I/O devices like typers and video display stations. Stand-alone keyboard and console configurations may also be specified. Regardless of physical location, the typical function of keyboards and consoles is to provide operator I/O communication with the digital process computer.

Because of hardware dependency, many keyboards and console functions are tested during the CPU subsystem test. In the case of I/O typers, video display stations, and other I/O devices with built-in keyboards, operation of the keyboard is verified at the same time the unit tests for these devices are run. Testing of special I/O consoles and keyboards supplied by independent vendors shall be negotiated and shall be in accordance with 2.6, Special Functions and 8.3.16, Special Functions.

All specified functions shall be tested. Typical keyboards and consoles may provide for:

- 1) Manual Entry of Data
- 2) Fetch or Inquiry of Stored Data
- 3) Program Status Indicators or Lamps
- 4) Timings and Basic Clocking Indicators or Lamps
- 5) Error Interlock Indicators or Lamps
- 6) Device Select or Sense Switches
- 7) Functional Keys and Switches

4.3.10.1 Keyboards

All keys, switches, and other similar functional hardware shall be tested in accordance with specifications. Typical keys and switches include:

- 1) Alphanumeric Keys
- 2) Special Character Keys
- 3) Space and Backspace Keys

- 4) Erase and Clear Keys
- 5) Reset Key
- 6) Power-On Switch
- 7) Mode Select Switch
- 8) Carriage Return Key
- 9) Fetch or Seek Key
- 10) Shift Key
- 11) Index Key
- 12) Tabulate Key

4.3.10.2 Consoles

All keys, switches, and other similar functional hardware shall be tested in accordance with specifications. Typical keys and switches include:

- 1) Program Sense Switch
- 2) Data Entry or Bit Select Switch
- 3) Mode Select or Device Select Switch
- 4) Clear Storage Key
- 5) Console Interrupt Switch
- 6) Operations Monitor Switch
- 7) Register Display Switch
- 8) Program Load Key
- 9) Start/Stop Key
- 10) Reset Key
- 11) Console Lockout Key

4.3.10.3 Indicators

All indicators shall be tested in accordance with specifications. Typical indicators include:

- 1) Ready Indicator
- 2) Power-On Indicator
- 3) Run or Busy Indicator
- 4) Wait, Halt, or Alarm Indicator
- 5) Error or Parity Indicator
- 6) Storage Protect Indicator
- 7) Instruction or Data Register Indicator
- 8) Interrupt Level Indicator

- 9) Cycle-Steal Indicator
- 10) Add/Subtract Indicator
- 11) Multiply/Divide Indicator
- 12) Overflow Indicator
- 13) Accumulator Sign Indicator
- 14) Clock Indicator
- 15) Instruction or Execute Indicator
- 16) Timer Indicator
- 17) Accumulator Register Indicators
- 18) Shift Register Indicators
- 19) Storage Address Register Indicators
- 20) Program Counter Indicators
- 21) Index Register Indicators

5 Recommended tests, digital inputs and outputs

5.1 Objective

The objective of these tests is to verify the basic parameters and specifications of the subsystem which typically include:

- 1) Addressing
- 2) Signal Level
- 3) Delay
- 4) Noise Rejection
- 5) Counting Accuracy
- 6) Timing Accuracy

5.2 Equipment to be tested

Digital input and output hardware, typically provided to connect digital process signals and communication devices to the computer system, shall be tested. This test does not include inputs or outputs associated with operator communication devices supplied by the vendor, other computers, or data processing peripherals included in 4, Data Processing Input-Output Subsystem. Testing the system response to hardware process interrupts is included in 3, Central Processing Unit. In this section, hardware process interrupts are considered as digital inputs and are tested accordingly.

The complete subsystem shall be tested as a unit with the bounds of the subsystem defined electrically as:

- 1) The field wiring connector or termination strip
- 2) The data word(s) at the subsystem data output bus
- 3) The control word(s) at the subsystem control bus
- 4) Power input to the subsystem.

5.3 Test procedures

5.3.1 Digital inputs

5.3.1.1 Addressing

This test shall be performed to verify digital input addressing. All digital inputs, including pulse and process interrupt inputs, shall be tested by connecting a signal to the input terminals and verifying that the input is detected at only the correct address.

5.3.1.2 Signal level

This test shall be performed using a specified number of voltage and contact inputs selected such that inputs are tested in at least two subgroups of each type.

5.3.1.2.1 Contact inputs

Verify that each input is detected with the maximum specified closed-contact resistance.

Verify that the input is not detected with the minimum specified open-contact resistance.

5.3.1.2.2 Voltage inputs

Verify that each input is detected with the minimum specified voltage for an input.

Verify that each input is not detected with the maximum specified voltage for no input.

5.3.1.3 Input delay

This test shall be performed using a specified number of voltage and contact inputs selected such that inputs are tested in at least two subgroups of each type.

Verify the minimum on-delay by applying a maximum signal level (such as minimum contact resistance or maximum specified input voltage) and measuring the delay before a signal appears on the data bus.

Verify the minimum off-delay by removing a minimum signal level (such as maximum contact resistance or minimum specified input voltage) and measuring the delay before a signal appears on the data bus.

Verify the maximum on-delay by applying a minimum signal level with the maximum specified source capacitance and inductance and measuring the delay before a signal appears on the data bus.

Verify the maximum off-delay by removing a maximum signal level with the maximum specified source capacitance and inductance and measuring the delay before a signal appears on the data bus.

5.3.1.4 Noise rejection

This test shall be performed using a specified number of voltage and contact inputs selected such that inputs are tested in at least two subgroups of each type.

On voltage and contact inputs, test for normal mode rejection by connecting a 60 Hz (or other frequency of interest) source of maximum specified magnitude to the digital input channel and verifying that no signal change appears on the data bus.

On differential inputs, test for common mode rejection by connecting a 60 Hz (or other frequency of interest) source of maximum specified magnitude from system ground to the digital input channel, and verifying that no signal change appears on the data bus. Repeat the test with the maximum specified dc common mode voltage.

5.3.1.5 Counting accuracy

This test shall be performed using a specified number of hardware pulse counters. Voltage and contact inputs shall be tested by generating a train of pulses with a solid-state switch, pulse generator, or other means.

Verify that pulses are counted accurately by generating a train of pulses equal to at least 50 percent of a single-word count value. If multiple words are used for the counter, the transfer of count between words shall be tested. Verify that the accumulated count is correct under the following two sets of conditions:

- 1) Maximum specified pulse rate, minimum specified peak input voltage, and minimum specified pulse width.
- 2) Maximum specified pulse rate, maximum specified peak input voltage, and maximum specified pulse width.

5.3.1.6 Overvoltage testing

If overvoltage protection is specified, this capability shall be tested by applying the maximum specified voltage to the input terminals and verifying the specified system response.

5.3.2 Digital outputs

5.3.2.1 Addressing

This test shall be performed to verify digital output addressing. All digital voltage and contact outputs shall be tested by addressing each channel and verifying that only the addressed output is actuated.

5.3.2.2 Power failure status

Power failure status shall be tested by verifying that no outputs change state or that all outputs switch to a defined state (if so specified) on a power failure, restoration of power, or other specified condition.

5.3.2.3 Signal level

This test shall be performed using a specified number of voltage and contact outputs selected such that outputs are tested in at least two subgroups of each type.

Verify that contact outputs and voltage outputs can drive the specified load by operating the maximum specified resistive-inductive-capacitive load with the maximum specified ac or dc voltage.

5.3.2.4 Output delay

This test shall be performed using a specified number of voltage and contact outputs selected such that outputs are tested in at least two subgroups.

Verify turn-on and turn-off delays by measuring the time between the command signal at the data bus and the change in state of the output.

5.3.2.5 Timing accuracy

This test shall be performed using a specified number of voltage and contact outputs if the timing is hardware controlled.

The duration of momentary outputs shall be measured by comparison to an independent timer to verify timing accuracy.

The duration of outputs whose timing, although hardware controlled, is specified under program control shall be tested by operating the output for times equal to 10, 50, and 90 percent of full scale and verifying that the operate time for each value is within the specified accuracy.

5.3.2.6 Pulse count accuracy

This test shall be performed using a specified number of pulse outputs if the number of output pulses is hardware controlled.

Verify the pulse count accuracy by operating the output for pulse counts equal to 10, 50, and 90 percent of full scale and verifying that the number of counts for each value is within the specified accuracy.

Verify that the pulse rate is within the specified accuracy by measuring the frequency of the output.

Verify that the pulse rise time, fall time, and width are within specification with the maximum specified load resistance, capacitance, and inductance.

6 Recommended tests, analog inputs

The testing of high accuracy analog subsystems requires care in the design and implementation of the tests if meaningful results are to be obtained. Errors due to phenomena such as ground loops or thermoelectric potentials can have a profound effect on test results. In addition, subsystem parameters are often defined differently by different vendors so that, for example, the term "accuracy" may have several definitions.

As a result, the tests recommended in this section are described in considerable detail to indicate the care with which the tests must be designed. Prior to the initiation of testing, it is strongly recommended that the vendor and user agree on definitions and testing procedures in the detail suggested by these recommended tests.

6.1 Objective

The objective of these tests is to verify the basic parameters and specifications of the subsystem which typically include:

- 1) Addressing
- 2) Sampling Rate

- 3) Accuracy
- 4) Linearity
- 5) Repeatability
- 6) Common Mode Rejection
- 7) AC Normal Mode Rejection
- 8) Input Resistance
- 9) Input Overload Response
- 10) DC Cross-talk
- 11) Common Mode Cross-talk
- 12) Gain-Changing Cross-talk

6.2 Equipment to be tested

The complete subsystem shall be tested as a unit with the bounds of the subsystem electrically defined as:

- 1) The field wiring connector or termination strip
- 2) The data word(s) at the subsystem data output bus
- 3) The control word(s) at the subsystem control bus
- 4) Power input to the subsystem

6.3 Test procedures

Temperature and humidity reference conditions as specified in the vendor specifications should be observed. If they are not, appropriate adjustments shall be made in the test specifications.

The equipment shall be allowed warm-up time as specified by the vendor.

The equipment shall be adjusted (such as power supplies and calibration) according to the vendor-specified adjustment procedure prior to testing. Readjustment shall be permitted during testing only if allowed in a specification or vendor-specified adjustment procedure.

The characteristics of the test equipment (such as accuracy and resolution) should be agreed upon by the vendor and user prior to the initiation of testing. This specifically includes agreement on the signal source to be utilized as the fundamental reference for accuracy and related measurements.

Voltage input signals should be used unless specified otherwise. In the case of a subsystem designed exclusively for current inputs, tests equivalent to those recommended may be used.

Several tests may be performed simultaneously when it can be shown that no interaction exists.

All tests shall be run at the maximum specified sampling rate unless another rate is specified.

6.3.1 Addressing test

This test is performed to verify that the subsystem addressing is correct and that one and only one input channel is selected for each address. This test shall be performed on all channels.

Connect an input signal equal to approximately 100 percent Full Scale (F.S.) to the first input channel and 50 percent F.S. to all other channels. Operate the subsystem to obtain one or more

readings on each channel and verify that the first channel reads approximately 100 percent F.S. and all other channels read approximately 50 percent F.S.

Move the 100 percent F.S. input signal to the next channel and connect the first input channel to the 50 percent F.S. input signal. Repeat the above test. Continue this procedure until all channels have been tested.

6.3.2 Sampling rate test

This test shall be performed to verify that the subsystem multiplexes, converts, and transfers data to the subsystem output bus at the maximum specified rate. This test may be run concurrently with any of the other tests which are run at the maximum specified rate.

The sampling rate of the subsystem may be measured either by means of software or the observation of logic signals in the subsystem (for example, "conversion complete" from the analog-to-digital converter (ADC)). Allowance should be made for normal software bookkeeping required in this test. This bookkeeping, in most cases, affects the average rate but not the instantaneous rate.

6.3.3 Accuracy tests

System accuracy can be defined in a number of ways. Appendix A, Analog Input Subsystem Accuracy, defines the criteria by which mean and total accuracy are calculated for the purposes of this standard. The tests described herein verify mean and total accuracy (including repeatability) over a specified time duration. It is not the intent of these tests to verify performance with respect to temperature or time as these are included in 8, Interacting Systems and 9, Environmental.

6.3.3.1 Mean accuracy test (single-gain subsystem)

The single-gain mean accuracy test shall be performed using a specified number of input channels having the specified source resistance.

An adjustable input signal source is connected to each input channel under test (a common source may be used if desired). The test is performed for input signal values from minus full scale to plus full scale in increments of approximately 20 percent of full scale. In subsystems designed for signals of a single polarity (unipolar subsystems), data collected for zero input signals may be statistically invalid. In this case, a near-zero input signal value should be used. An input signal of approximately 1 percent F.S. is recommended.

The subsystem shall be operated to collect a statistically significant number of readings for each input signal value. A distribution analysis of the readings shall be made either by the computer or manually. The mean value $\bar{x}$, mean error E , and mean accuracy A are calculated as described in A.3.2.

6.3.3.2 Total accuracy (single-gain subsystem)

The test shall be performed using a specified number of input channels having a specified source resistance. The test conditions are the same as for the mean accuracy test. Data collected for the mean accuracy test may be used for the total accuracy calculations.

The maximum error $E_{\max}$ and total accuracy A_{tot} are calculated as described in A.3.3.

6.3.3.3 Multiple gain accuracy tests

On systems having gain-changing capability or other forms of multiple gain, the mean and total accuracy tests shall be performed on all gains. On one selected gain, the tests shall be conducted as described in 6.3.3.1, Mean Accuracy Test and 6.3.3.2, Total Accuracy. On the

remaining gains, the same tests shall be performed except that the input may be varied in increments of 50 percent of full scale from minus full scale to plus full scale.

6.3.4 Linearity test

The linearity error is evaluated over the total number of input signal values using the data collected for the mean accuracy test. The calculation is valid for unipolar and bipolar systems.

The linearity error L is calculated as described in A.4.

6.3.5 Repeatability test

Repeatability is evaluated for each input signal value using the data collected for the mean accuracy test. For the purpose of this standard (See A.2.2), repeatability R_m is:

$$R_m = \pm \text{Max}(R_1, R_2)$$

where

$$R_1 = x_{\max} - \bar{x}$$

$$R_2 = \bar{x} - x_{\min}$$

$x_{\max}$ = effective maximum output reading (such as maximum output reading after 0.3 percent of the samples may have been discarded)

$x_{\min}$ = effective minimum output reading (such as minimum output reading after 0.3 percent of the samples may have been discarded)

$\bar{x}$ = mean value of the distribution of readings

Repeatability is typically expressed as a percentage of full range (percent F. R.) according to the expression.

$$R = (R_m/x_{F.R.}) 100$$

where $x_{F.R.}$ is the full range value.

6.3.6 Common Mode Rejection (CMR)

This test is performed at each subsystem gain to verify the effect of a common mode voltage (CMV) applied to the input channel.

This test shall be performed using a specified number of inputs selected such that the block of inputs shall overlap at least one submultiplexer boundary if one exists in the subsystem.

Connect a signal source having a value of approximately 50 percent of full scale to each input. The signal source resistance and unbalance. The unbalance may be in either the low (negative) or high (positive) side of the input unless a specific configuration is defined in the subsystem specifications. In Figure 6.1, R_{s_1} and R_{s_2} indicate both the source resistance (R_s) and line unbalance (R_u) according to the equations:

$$R_s = R_{s_1} + R_{s_2}$$

$$R_u = |R_{s_1} - R_{s_2}|$$

The signal source should be referenced to the system ground unless another reference point is specified. The input cable shield (if present or required) should be connected according to the subsystem specification or the recommended practice of the vendor.

A statistically significant number of output readings is collected from each input channel. The mean value of the readings referred to the input (RTI) is calculated for each input channel according to the formula in A.3.2 (in subsequent calculations, this value is denoted by $\bar{x}_1$). In addition, the spread of readings RTI is recorded for each input (in subsequent calculations, this value is denoted by S_1).

A CMV source then shall be connected between each input and the point to which the input signal sources were originally referenced (usually system ground). A single CMV source may be used for all input channels. [Figure 6.1](#) illustrates a typical test configuration for a single channel.

For the determination of the dc CMR performance, the CMV source is adjusted to the specified maximum dc CMV. A statistically significant number of readings is collected and their mean value RTI calculated according to the formula in [A.3.2](#).

The dc CMR in decibels (dB) is calculated for each input channel according to the equation:

$$\text{dc CMR} = 20 \log_{10} \left| \frac{\text{CMV}}{\bar{x}_1 - \bar{x}_2} \right| \text{dB}$$

where

CMV = applied CMV (dc volts)

$\bar{x}_1$ = mean value of output readings RTI (volts) without CMV applied

$\bar{x}_2$ = mean value of output readings RTI (volts) with CMV applied.

For the determination of the ac CMR performance, the CMV source is adjusted to the specified maximum peak-to-peak value. A statistically significant number of readings is collected from each input channel. The spread of readings RTI is determined according to the equation:

$$S = R_1 + R_2$$

where R_1 and R_2 are defined in A.2.2

$$\text{ac CMR} = 20 \log_{10} \left| \frac{\text{CMV}}{S_1 - S_2} \right| \text{dB}$$

where

CMV = applied CMV (volts peak-to-peak)

S_1 = spread of output readings RTI (volts peak-to-peak) without CMV applied

S_2 = spread of output readings RTI (volts peak-to-peak) with CMV applied.

The ac CMR should be tested at the nominal power line frequency. To determine frequency sensitivity, ac CMR may be tested at frequencies slightly greater than, and slightly less than, the nominal power line frequency. A variation of approximately ± 5 Hz is recommended.

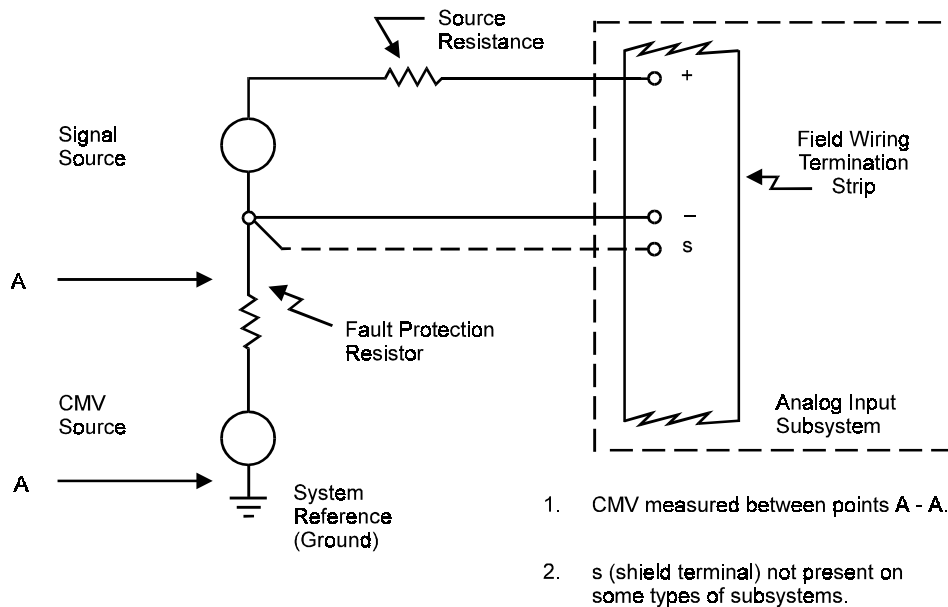


Figure 6.1 — Typical CMR test configuration

(Shown for only one input channel)

To insure consistent results, the ac CMV signal wave form should be as free of distortion as possible.

In subsystems whose CMR depends on synchronization with the power line frequency, care may be required in selecting the ac CMV source. If such synchronization is required, it should be specified by the vendor.

In subsystems having very high CMR or a low value of allowable CMV, the differences ($\bar{x}_1 - \bar{x}_2$) and ($s_1 - s_2$) may not be statistically significant. In this case, the CMR may be stated as being greater than the value obtained when the value of the quantizing interval RTI is substituted for the difference terms in the CMR equations.

6.3.7 AC normal mode rejection (ac NMR) test

This test shall be performed to verify the effect of ac voltage in series with the signal source.

Tests shall be performed using a specified number of input channels. If a variety of signal conditioning (such as filters) or other options having frequency-dependent characteristics are provided in the subsystem, the selection of input channels shall include at least one channel equipped with each option.

This test may be performed at only one gain unless the gain characteristics are frequency dependent within the range of the test frequencies.

A signal source consisting of a dc source connected in series with an ac source is connected to each of the selected channels. A common source may be utilized for all channels. The signal source shall be referenced to the system ground unless another signal reference point is specified. Input shields, if present, should be connected according to the subsystem specifications or the recommended practice of the vendor. The test configuration is shown in [Figure 6.2](#) for one input channel.

A statistically significant number of readings is collected from each input channel under the following conditions and the spread of the distribution is recorded in each case.

- 1) DC signal source adjusted to 50 percent F.S. with the ac signal source short-circuited. (The observed value of the spread RTI is denoted as S_1 in subsequent calculations.)
- 2) DC signal source adjusted as in (1) with the ac signal source adjusted to a value such that the sum of the dc signal and the peak ac value does not exceed the specified maximum allowable input signal amplitude. (The observed spread RTI is denoted as S_2 in subsequent calculations.) The ac signal frequency should be equal to the nominal power line frequency.

In order to determine frequency sensitivity, data may be collected with the frequency of the ac source adjusted to slightly greater than, and slightly less than the nominal power line frequency. The suggested variation is approximately ± 5 Hz.

The ac normal mode rejection ac NMR in dB for each input channel and test condition specified in (2) is calculated from the equation:

$$\text{ac NMR} \equiv 20 \log_{10} \left| \frac{V_{\text{ac}}}{S_2 - S_1} \right| \text{dB}$$

where

S_1 = spread RTI (volts) as obtained from case (1)

S_2 = spread RTI (volts) as obtained from case (2)

V_{ac} = applied peak-to-peak ac signal (volts)

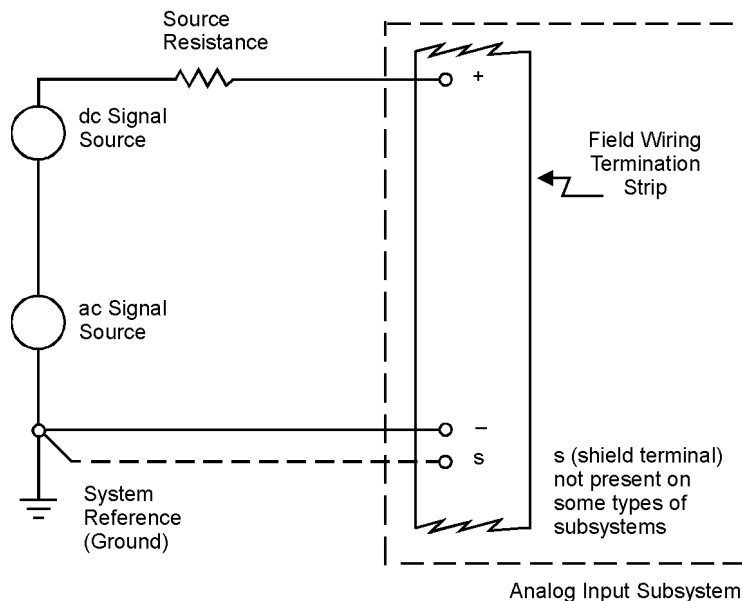


Figure 6.2 — Typical NMR test configuration
(Shown for only one input channel)

The ac signal waveform should be as free of distortion as possible to obtain consistent results.

In subsystems whose ac NMR depends on synchronization with the power line frequency, the selection of the ac signal source may require special consideration. If such synchronization is required, it should be specified by the vendor.

In subsystems having very high NMR, it may not be possible to measure a statistically significant $(S_2 - S_1)$ within the maximum allowable input voltage specification. In this case the quantity $(S_2 - S_1)$ may be replaced by the quantizing interval RTI and the ac NMR stated as being greater than the value determined from $\text{ac NMR} = 20 \log_{10} (V_{\text{ac}}/Q)$ where Q is the quantizing interval.

6.3.8 Effective input resistance test

This test shall be performed at maximum subsystem gain to verify the specified input resistance of the subsystem. The test is applicable only to systems designed for voltage input signals.

This test should be performed using a small number of input channels.

One test method is based on observing the loading effect of the signal source resistance. The following recommended test is based on this method.

Connect a voltage input source equal to approximately 100 percent F.S. to each selected input channel. The resistance of the input signal source should be adjustable between the maximum and minimum specified source resistance of the subsystem.

Operate the subsystem to collect a statistically significant number of readings from each input channel in the following cases:

- 1) Source resistance set to its minimum value. For this case, the source resistance in ohms is designated as R_a and the mean value of the output readings calculated using the formula in A.3.2 for each input channel is designated as $\bar{x}_1$.
- 2) Source resistance set to its maximum value. For this case, the source resistance in ohms is designated as R_b and the mean value of the output readings for each input channel is designated as $\bar{x}_2$.

The effective input resistance R_{eff} is calculated from:

$$R_{\text{eff}} = (R_b \bar{x}_2 - R_a \bar{x}_1) / (\bar{x}_1 - \bar{x}_2) \text{ ohms}$$

Example:

$$R_a = 10 \text{ ohms} \quad \text{Mean output value} = \bar{x}_1 = 10.00 \text{mv}$$

$$R_b = 1000 \text{ ohms} \quad \text{Mean output value} = \bar{x}_2 = 9.99 \text{mv}$$

$$R_{\text{eff}} = (9990 - 100) / (0.01) = 989,000 \text{ ohms}$$

This test measures the net effect of input resistance (which obeys Ohm's Law), offset current, and other effects which may be independent of applied voltage. As a result, the measured effective input resistance may be a function of input voltage.

The effective input resistance may be a function of the sampling rate for a given channel. If specified, the maximum per channel rate shall not be exceeded. If not specified, any rate not exceeding the maximum specified system sampling rate may be used.

On subsystems having very high input resistance, low resolution, or other limitations, the difference between $\bar{x}_1$ and $\bar{x}_2$ may not be statistically significant. In this case, the effective input resistance can be stated to be greater than the value obtained using the formula when $(\bar{x}_1 - \bar{x}_2)$ is set equal to the quantizing interval.

6.3.9 Input overload response test

This test shall be performed to determine the effect on succeeding channels of an overloaded channel (where the input signal exceeds the specified full scale signal).

A testing approach is to observe the effect of an overloaded channel on the output readings of subsequent channels. It is difficult to separate the effects of overload recovery and dc cross-talk when certain gain combinations are used on successive channels (e.g., minimum gain followed by maximum gain). This fact should be considered in interpreting the results of the following recommended test procedure.

This test shall be performed on three adjacent input channels. These channels should be contained in the same submultiplexer group. For the purposes of this test, these channels are designated as Channels 1, 2, and 3.

In collecting data, the three channels are read repeatedly in consecutive order at the maximum system sampling rate. The sampling rate on any particular channel, however, shall not exceed the maximum per-channel sampling rate if such a rate is specified. It may be necessary to cause a delay between reading Channel 3 and Channel 1.

The gain of each channel is set to its maximum specified value. An input signal source having the maximum specified source resistance and adjusted to approximately 50 percent F.S. is connected to the input channels. A common signal source may be utilized for Channels 2 and 3.

The signal sources shall be referenced to system ground unless an alternate reference point is specified.

The following data collection and processing are then performed:

- 1) A statistically significant number of readings is collected from Channels 2 and 3 and the mean value of the output readings RTI is calculated according to the formula in A.3.2.
- 2) The value of the input signal on Channel 1 is increased to the maximum allowable overload value and (1) is repeated.
- 3) The overload recovering effect E_o is calculated as a percentage of the overload signal for each channel as follows:

$$E_o = (\bar{x}_1 - \bar{x}_2) / x_0 \times 100$$

where:

$\bar{x}_1$ = mean value of output readings RTI determined in (1)

$\bar{x}_2$ = mean value of output readings RTI determined in (2)

x_0 = value of overload signal on Channel 1

If the overload error on Channel 3 is substantial, the test may be repeated using more than three channels to observe the number of additional channels substantially affected by the overload condition.

- 4) In subsystems providing multiple gain capability within a submultiplexer group, (2) and (3) may be repeated for all available gains of Channel 1. If the maximum allowable overload voltage is a function of the gain setting, the overload voltage applied to Channel 1 is adjusted accordingly. The gain settings of Channel 2 and 3 shall remain at their maximum values.
- 5) In subsystems providing only a single gain within a submultiplexer group, (1) through (3) may be repeated for each available gain.

6.3.10 DC cross-talk test

This test shall be performed to determine the error on one input channel caused by an input signal on an adjacent input channel.

The recommended procedure for this test is identical to that used to determine the overload effect described in 6.3.9, Input Overload Response Test, with the exception that, in (2), the input signal on Channel 1 is adjusted to approximately 100 percent F.S. Its value is designated as $x_{F.S.}$.

The error as a percentage of $x_{F.S.}$ is calculated as described in 6.3.9 or in decibels according to the expression:

$$\text{Crosstalk} = 20 \log_{10}(x_{F.S.}/|x_1 - x_2|) \text{dB}$$

where the parameters x_1 and x_2 have the same meaning as defined in 6.3.9.

Although three channels are recommended in the test, a larger number may be required depending on physical layout, wiring proximities, etc.

6.3.11 Common mode cross-talk test

This test shall be performed to verify the effect on one channel caused by common mode voltage applied to an adjacent channel.

The recommended test conditions and method for this test are identical to the Common Mode Rejection Test in 6.3.6, Common Mode Rejection, with the following exceptions:

- 1) The input channels selected for the test shall be adjacent channels and included in the same submultiplexer group.
- 2) The common mode voltage source is connected to only the first of the selected channels.
- 3) The input channels are samples in a sequential order in a manner similar to that specified in 6.3.9, Input Overload Response Test.
- 4) Collect and process data for the two channels immediately following the channel to which the common mode source is applied.
- 5) The parameters used in the calculation of the CMR in 6.3.6 have the same meaning except that they apply to the data collected as described in (4) above. The rejection factor calculated from the formula in 6.3.6 is referred to as the Common Mode Cross-talk Rejection.

6.3.12 Gain-changing cross-talk test

On systems having gain-changing capability, a test shall be performed to determine gain-change settling characteristics between adjacent channels.

The test configuration and sampling sequence for this test are identical to that used for the Input Overload Test (6.3.9).

- 1) A statistically significant number of readings is collected from Channels 2 and 3 with the input signals to Channels 1, 2, and 3 being adjusted to approximately 50 percent F.S. and maximum gain settings. The mean value of the readings RTI for Channels 2 and 3 is calculated according to the formula given in A.3.2. This mean value for each input channel is denoted as x_1 .

- 2) The gain of Channel 1 is reduced to its minimum value and data are collected and processed as in the previous step. The mean value for each input channel is denoted as $\bar{x}_2$.
- 3) The mean error due to gain-changing cross-talk is calculated using the formula for mean error in A.3.2.

In many systems, this measurement results in a difference in the means $\bar{x}_1$ and $\bar{x}_2$ which is statistically insignificant compared to the system resolution. In this case, the error can be defined as negligible.

6.3.13 Special features

Testing methods of special subsystem features not covered by this standard shall be negotiated by the vendor and user before the system is contracted.

Examples of special features for analog input subsystems are:

- Overvoltage protection
- Open circuit detection
- Sample-and-hold amplifiers
- External synchronization

In addition, tests relative to aliasing errors are not included in the standard. These errors are a function of input signal frequencies generated outside the boundaries of the Analog Input Subsystem.

7 Recommended tests, analog outputs

The testing of analog output subsystems should be considered in a manner similar to that described in the preface to 6, Analog Inputs.

7.1 Objective

The objective of these tests is to verify the basic parameters and specifications of the subsystem which typically include:

- 1) Addressing
- 2) Accuracy
- 3) Output Capability
- 4) Capacitive Loading
- 5) Noise
- 6) Settling Time
- 7) Cross-talk
- 8) Droop Rate for Sample-and-Hold Output Channels

7.2 Equipment to be tested

The complete subsystem shall be tested as a unit with the bounds of the subsystem defined electrically as:

- 1) The field wiring connector or termination strip
- 2) The data word(s) at the subsystem data output bus
- 3) The control word(s) at the subsystem control bus
- 4) Power input to the subsystem

7.3 Test procedures

Temperature and humidity reference conditions as specified by the vendor should be observed. If they are not, appropriate adjustments shall be made in the test specifications.

The equipment shall be allowed warm-up time as specified by the vendor.

The equipment shall be adjusted (such as power supplies and calibration) according to the vendor-specified adjustment procedure prior to testing. Readjustment shall be permitted during testing only if allowed in a specification or vendor-specified adjustment procedure.

The characteristics of the test equipment (such as accuracy and resolution) should be agreed upon by the vendor and user prior to the initiation of testing. This specifically includes agreement on the signal source to be utilized as the fundamental reference for accuracy and related measurements.

The analog input subsystem may be utilized as a measuring instrument in these tests if its specifications are adequate.

7.3.1 Addressing test

This test is performed to verify that the subsystem addressing is correct and that one and only one output channel is selected for each address. This test shall be performed on all channels.

One output is adjusted to approximately 50 percent F.S. with all other channels adjusted to zero output.

The output of all channels shall be measured to determine that only the addressed channel has been selected. The test is repeated for all channels with each channel being addressed separately.

7.3.2 Mean accuracy test

This test shall be performed using a specified number of analog output channels connected to the specified load. The test shall be run on one output channel at a time and repeated for each of the selected channels. In subsystems having output channels capable of providing outputs of both positive and negative polarity, the procedure shall be repeated for both polarities.

A suitable measuring device is connected to the field wiring connector or termination strip of the channel being measured. If the analog input subsystem is used, measurements shall be based on the mean value of a statistically significant number of readings in accordance with A.3.1.1.

As described below, there are minor variations in the test depending on whether binary-coded or binary-coded-decimal digital inputs are utilized. The following data collection and processing are performed:

7.3.2.1 Binary-coded subsystem

- 1) On the channel being tested, each bit is energized separately. The mean errors of the corresponding output shall be determined. In the binary-coded subsystem, the digital input values would be 0001, 0010, 0100, etc.
- 2) Energize all bits which exhibited a positive error in the above procedure and measure the mean value of the resulting output.
- 3) Calculate the error E according to the expression in A.3.2.
- 4) Repeat the measurement with all bits which exhibited a negative error being energized.
- 5) Again calculate the mean error.
- 6) Calculate mean accuracy A according to the expression in A.3.2. Although it is common practice to use the mean error as an indication of system accuracy, a more correct method is to utilize the results of the mean accuracy equation, which would give 99.9 percent full range (F.R.) accuracy if the mean error is 0.1 percent F.R.

7.3.2.2 Binary-coded-decimal subsystem

- 1) On the channel being tested, each digit is energized separately. The mean errors of the corresponding output shall be determined. In a binary-coded-decimal subsystem, the digital input values would be 0001, 0002, . . . , 0009, 0010, 0020, . . . , 0090, etc.
- 2) For each digit position in the input word, energize the digit in each digit position which exhibited the maximum positive error in the above procedure and measure the mean value of the resulting output value.
- 3) Calculate the mean error according to the expression in A.3.2.
- 4) Repeat the measurement using the digit in each digit position which exhibited the maximum negative error.
- 5) Again calculate the mean error.
- 6) Calculate the mean accuracy A according to the expression in A.3.2.

7.3.3 Output capability test

This test shall be performed using a specified number of output channels.

The output capability of an analog output channel is a measure of its ability to deliver a specified voltage or current to a specified load.

7.3.3.1 Voltage output channel

Two methods of specifying voltage output channels are:

- 1) The maximum output current or the minimum load may be specified. Unless otherwise specified, it may be assumed that the mean value of the output voltage remains within the specified mean error (accuracy) specification over the range of allowable output current or, equivalent, the range of output load resistance.
- 2) The voltage regulation as a percentage of full range output or the voltage change as the load varies from a minimum to a maximum value may be specified. Unless otherwise specified, it may be assumed that the regulation error is in addition to a specified mean error.

A load which is variable within the specified limits or implied by the current specification is connected to the selected output channel. The voltage output of the channel is adjusted to its maximum value and the load resistance is adjusted to its minimum value, denoted by R_A . The mean value of the output voltage shall be measured and is denoted as $\underline{x}_1$. The load is then adjusted to its maximum specified value (which may be infinite) and the mean value of the output shall be measured. This value is denoted as $\underline{x}_2$ with the corresponding resistance denoted as R_B .

Depending on the manner in which the channel capability is specified, one of the following calculations shall be made:

- 1) Verify that the maximum output current is available using the value of $\underline{x}_1$ and the minimum resistance value R_A according to Ohm's law: $I = \underline{x}_1/R_A$. Calculate the mean error at maximum and minimum current levels according to the equation in A.3.2.
- 2) Calculate the voltage regulation expressed in percent full range (percent F.R.) according to the equation:

$$\text{Regulation} = \left(\frac{\underline{x}_2 - \underline{x}_1}{x_{\text{F.R.}}} \right) \times 100$$

where $x_{\text{F.R.}}$ is the nominal full range output voltage.

7.3.3.2 Current output channel

Two methods of specifying current output channels are:

- 1) The maximum output voltage or the maximum allowable load resistance may be specified. Unless otherwise specified, it is assumed that the mean value of the output current remains within the specified mean error (accuracy) specification over the allowable range of output voltage or, equivalently, the range of output load resistance.
- 2) The current regulation as a percentage of full range output or the current change as the load varies from maximum to minimum may be specified. Unless otherwise specified, it may be assumed that the regulation error is in addition to the specified mean error.

A load which is variable within the specified limits or implied by the voltage specification is connected to the selected output channel. The output current of the channel is adjusted to its maximum value and the load resistance is adjusted to its minimum value, denoted as R_A . The mean value of the output voltage shall be measured and is denoted as $\underline{x}_1$. Alternately, the mean value of the output current may be measured directly and the subsequent equations altered accordingly. The load resistance then is adjusted to its maximum value which is denoted by R_B . The mean value of the output voltage, denoted by $\underline{x}_2$, shall be measured.

Depending on the manner in which the channel capability is specified, one of the following calculations shall be made:

- 1) Verify that the maximum output voltage is available by comparing $\underline{x}_2$ and R_A to the specified values. Calculate the mean error 3 expressed in percent full range (percent F.R.) from the equation.

$$E = \frac{(\underline{x}_1 - R_B I_{\text{F.R.}})}{R_B I_{\text{F.R.}}} \times 100$$

where $I_{F.R.}$ is the full range output current.

- 2) Calculate the current regulation expressed in percent full range (percent F.R.) according to the equation:

$$\text{Regulation} = \frac{R_B X_1 - R_A X_2}{R_A R_B I_{F.R.}} \times 100$$

If $R_A = 0$, this equation cannot be utilized.

The regulation can be calculated, however, if a direct measurement of the short-circuit ($R_A = 0$) current is made. If the value of this current is denoted by I_A , the regulation expressed in percent full range (percent F.R.) is:

$$\text{Regulation} = \frac{R_B I_A - X_2}{R_B I_{F.R.}} \times 100$$

Another way of expressing regulation is:

$$\text{Regulation} = \frac{I_A - I_B}{I_{F.R.}} \times 100$$

where I_B is output current when R_A is maximum.

7.3.4 Capacitive loading test

This test shall be performed using a specified number of output channels. The selected channels are connected to the specified resistive load and adjusted for an output value of approximately 10 percent F.S. The outputs are observed with an oscilloscope having a bandwidth greater than the frequency range of interest. Capacitance is added in parallel with the resistive load in steps of approximately 20 percent of the maximum specified value. The output shall be observed to determine if noise or oscillations in excess of those specified are present.

The test shall be repeated with the output channels adjusted for an output value of approximately 100 percent F.S. Channels providing output of both polarities shall be tested using output values of both polarities.

If combination limits of resistance and capacitance are specified, the above test may be modified to provide for the variation of both the resistance and capacitance values. If limits on load inductance are specified, a test analogous to that described in this section shall be performed.

7.3.5 Noise test

This test shall be performed on a specified number of output channels.

Each output channel is connected to the specified resistive load.

The selected channels are adjusted for an output value of approximately 50 percent F.S. The output noise is measured over a specified bandwidth as determined by a single-section RC filter using an rms voltmeter. [Figure 7.1](#) illustrates a typical test configuration for a single output channel.

The rms voltmeter must have a bandwidth significantly greater than that of the filter. In addition, it must have the capability of accurately measuring the rms voltage in the presence of the dc voltage of the output channel.

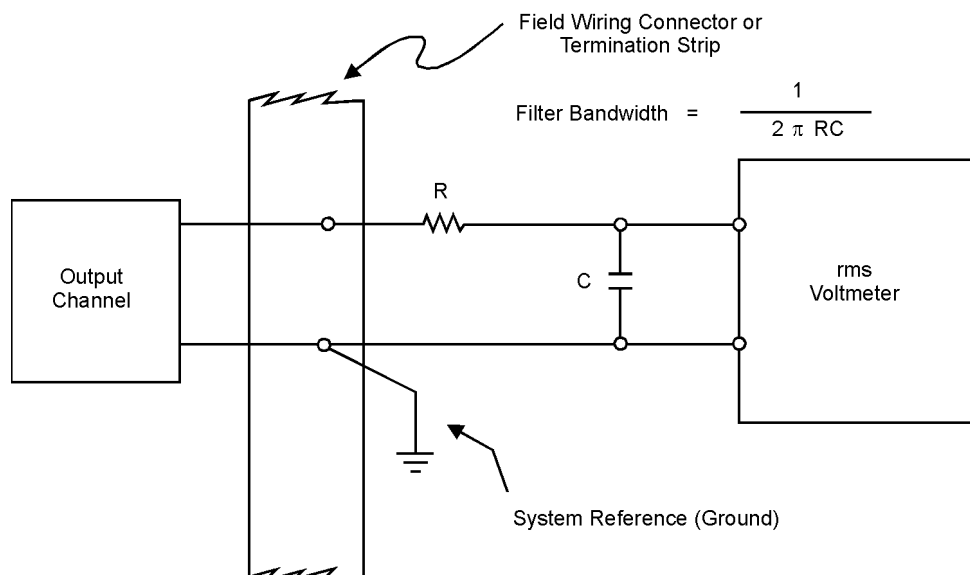


Figure 7.1 — Noise measurement test configuration

7.3.6 Settling time test

This test shall be performed using a specified number of output channels. Each output channel is connected to the specified resistive load. An oscilloscope or other suitable instrumentation is connected to the output. The instrumentation must be capable of simultaneously monitoring or displaying the digital signal which initiates a change in the output channel value as well as the output signal. The output channel is controlled to periodically switch the output value between specified limits. If no specific values are specified, the extremes of the output range shall be used.

The settling time is measured as the maximum time elapsed from the initiation of the digital signal until the analog output value stays within a band, specified as a percentage of the full scale output value, of the output signal.

The test shall be repeated with the output channel connected to the maximum specified capacitive load.

In high precision analog output subsystems, this may be a difficult test to perform if the settling time is small. Due to the resolution required in the measurement, an instrument utilizing an offset (zero suppression or expanded scale) technique usually is required. Care must be exercised in the selection of the equipment to insure that the transient produced in the instrument by the rapid change in the input voltage does not affect its ability to measure the output value with the required precision.

7.3.7 Cross-talk tests

7.3.7.1 DC cross-talk

This test shall be performed to determine the effect of a change in output of one output channel on the output value of an adjacent output channel.

The test shall be performed using two adjacent output channels. Each channel is connected to the specified resistive load. A suitable measuring device is connected to the output.

The output of Channel 2, the channel of interest, is adjusted to a value of approximately 50 percent F.S. Channel 1 is adjusted to a value of approximately 0 percent F.S.

The following data collection and processing are then performed:

- 1) The mean value of the output of Channel 2, noted as $\bar{x}_1$, is measured. If the analog input subsystem is used for this measurement, the mean value is calculated.
- 2) The value of the output signal on Channel 1 is increased to approximately 100 percent F.S. and (1) is repeated with the mean value of Channel 2 now denoted as $\bar{x}_2$.

The cross-talk error E_{CT} as a percentage of full scale is calculated according to the equation:

$$E_{CT} = \left(\frac{\bar{x}_1 - \bar{x}_2}{x_{F.S.}} \right) \times 100$$

- 3) where $x_{F.S.}$ is the full scale output value. DC cross-talk may be calculated in decibels (dB) according to the expression:

$$\text{DC cross-talk} = 20 \log_{10}(x_{F.S.}/|\bar{x}_1 - \bar{x}_2|) \text{ dB}$$

7.3.7.2 AC cross-talk

This test shall be performed using one output channel selected within a specified group of output channels.

To test for ac or transient cross-talk, each channel in the group is connected to a specified resistive load. All channels are adjusted for zero output. Using an oscilloscope or other suitable instrumentation, the selected channel shall be observed for oscillations and noise.

All channels, except the selected one, are then programmed to switch between the extremes of the full scale at the maximum rate. The selected channel is observed to determine if any increase in oscillations or noise is within specified limits.

7.3.8 Droop rate test

The droop rate is a measure of the time dependency of the output. This parameter is applicable typically to systems where the final output unit is a sample-and-hold element (analog memory).

This test shall be performed using a specified number of output channels equipped with this function.

The output channel is adjusted to approximately 100 percent F.S. and the mean value of the output is measured while the channel is in the sample mode. The mean value is denoted as $\bar{x}_1$.

Switch the output channel from the sample mode to the hold mode and simultaneously trigger a time-measuring device such as a counter, oscilloscope, or stopwatch.

After a specified period of time T , measure the mean value of the output, denoted as $\bar{x}_2$. If a time period T is not specifically stated, it is suggested that its value in seconds be determined from the equation $T = 10E/DR$ where DR is the droop rate specification in volts/second (or mA/S) and E is the specified mean error of the output in volts (or mA).

The droop rate is calculated using the equation:

$$DR = \frac{\bar{x}_1 - \bar{x}_2}{T} \text{ volts/sec (or mA/S)}$$

If specified in terms of a percentage of full scale, the droop rate is calculated using the equation:

$$DR = \frac{x_1 - x_2}{x_{F.S.} T} \times 100 \text{ percent F.S./sec.}$$

where $x_{F.S.}$ is the full scale output value in volts (or mA).

The calculations described for this recommended test are based on the assumption that the droop is a linear function of time. In reality, the function is usually an exponential decay. The described procedure, however, is usually valid for output channels designed to have a small droop over a time period which is short compared to the exponential time constant of the droop function.

7.3.9 Special Features

Testing methods of subsystem features not covered by this standard shall be negotiated by the vendor and user before the system is contracted.

Examples of special features for analog output subsystems are as follows:

- 1) Predictable action on power failure
- 2) External synchronization
- 3) Multiplying capability

8 Recommended tests, interacting system

8.1 Objective

The interacting system test shall determine that there are no detrimental interactions from concurrent operation of previously proven separate subsystems. Therefore, before starting the interacting system test, it is assumed that all subsystems have been individually tested, accepted, and calibrated. The following procedure provides the opportunity for random occurrence of interactions rather than predetermining specific interactions.

The interacting system test shall demonstrate the capability of the total vendor-supplied system to operate in a simulated real-time environment similar to that encountered in the planned application of the system.

8.2 Equipment to be tested

All subsystems including vendor supplied cables where available, shall be tested as a total system.

Subsystems and their functions to be tested may include:

- 1) Analog input
- 2) Digital input
- 3) Pulse input
- 4) Analog output

- 5) Digital output
- 6) Bulk Storage
- 7) Main storage
- 8) Arithmetic and control
- 9) Paper tape and card punches and readers
- 10) Typers and line printers
- 11) Hardware process interrupt
- 12) Hardware timers
- 13) Consoles
- 14) Data collection terminals and data modems
- 15) Hardware storage protection
- 16) Special functions

8.3 Test procedures

A program is necessary to supervise and coordinate each of the subsystem testing routines. If the system capability exists, this program shall approach concurrent execution of routines under interrupt control and provide a means of establishing priorities. Typical routines are listed in B.1.

When available and consistent with individual subsystem specifications, digital inputs and outputs may be interconnected to perform some tests. Similarly, analog inputs and outputs may be interconnected. The evaluation of subsystem performance must account for the summation of output and input errors.

Factors which must be considered on a pre-system basis include system configuration, quantity and addresses of multiple channels or devices in a subsystem, priority assignment of each subsystem, functions to be tested, time duration for each subsystem test, and the total time duration of the interacting system test. Enough time should be allowed for the interacting system test to provide a reasonable opportunity for interaction to occur. Factors affecting test duration are listed in B.2. The system specifications determining out-of-limit conditions shall be the subsystem specifications unless separate system specifications are defined. The following abbreviated tests shall approach concurrent operation on a non-periodic basis whenever possible. Any tests specifying operation of a subsystem at its maximum rate shall be interpreted as meaning the maximum rate consistent with the requirement for near concurrent operation.

Perform the applicable portions of the following interacting system test for the specified period and then examine the data to determine whether to extend, rerun, or terminate the test based on explanation of any failures. Errors or failures caused by the operator or program or by other than system hardware malfunctions shall not be counted against the system. Any detected error shall cause an automatic printout and an operation summary shall be printed periodically. If automatic printout is not permitted by the nature of the detection (such as visual), the error should be manually recorded.

8.3.1 Analog inputs

The analog input channels, less those connected as specified in 8.3.5, Analog Outputs, or, if not practical for very large systems, a lesser number of analog inputs, should be divided into groups for connection to different reference voltage sources (including a zero voltage source). If possible, these inputs shall be read in a sequence which causes successive readings to be at

different voltage levels. The inputs shall be read aperiodically at the maximum specified rate and a histogram obtained for each voltage level. The computer shall print out the input channel address and the value of any reading which is out of specified limits. Overflow indication shall be recorded. System accuracy and repeatability are the parameters to which the system shall be tested. The histogram printout shall be logged periodically or on demand and shall be summarized for the period of the test.

B.3 lists an optional use of the histogram as a qualitative diagnostic aid, although it is not generally applicable as a pass-fail criterion. [See Appendix A](#) for analog sub-system accuracy, repeatability calculations, and time and temperature dependence.

8.3.2 Digital inputs

A specified number of digital inputs shall be read in a pre-determined pattern at the maximum specified rate. The data shall be compared to the original pattern to detect errors.

8.3.3 Pulse inputs

Inputs to the hardware pulse counters shall be generated and then verified through an independent means. The contents of these pulse counters shall be printed periodically and examined to verify that the correct number of counts has been accumulated.

8.3.4 Digital outputs

A specified number of digital outputs shall be operated in a pre-determined pattern and monitored for error detection.

8.3.5 Analog outputs

A specified number of analog outputs shall generate values which shall vary in one count and random increments from zero to full scale value. The analog outputs shall be read and compared with the values that were to be generated. [See Appendix A](#) for analog sub-system accuracy calculations, and time and temperature dependence.

8.3.6 Bulk storage

Read and write data at the maximum specified rate from and to a storage area greater than one computer word and test for correct transfer.

8.3.7 Main storage

Read and write known data at the maximum specified rate from and to main storage not being used by test programs and test for correct transfer.

8.3.8 Arithmetic and control

Aperiodically execute the complete complement of instructions to verify their proper operation. This shall be accomplished executing an algorithm which provides for the comparison of the actual and expected results.

8.3.9 Paper tape and card punches and readers

Punch a known pattern and read the same pattern on an aperiodic basis. Error detection is accomplished by comparing the punched and read patterns.

8.3.10 Typers and line printers

Print the full complement of characters on an aperiodic basis. Verify applicable line spacing, tab, return, and other functions.

8.3.11 Hardware process interrupt

Aperiodically test operation of the external interrupts using a suitable means for producing external interrupt signals.

8.3.12 Hardware timers

Aperiodically test all hardware timers and print their contents to verify proper time operation. Aperiodically inhibit resetting the watchdog timer and verify that the specified alarm action occurs.

8.3.13 Consoles

Aperiodically operate consoles as they are normally used on-line to verify proper system response.

8.3.14 Data collection terminals and data modems

Connect terminal or modem outputs to the inputs and aperiodically send and receive messages to verify proper operations. Half-duplex configurations may require that this test be omitted unless other equipment is available. A pseudorandom pattern generator of a specified length may be utilized in determining error performance.

8.3.15 Hardware storage protection

Aperiodically test this function by executing programs in a certain area of main storage in the protected mode and try to write into this protected area. This shall result in the specified violation signal, indicator, or interrupt. The test shall verify that data in the protected area were not modified by the attempt to write into that area.

8.3.16 Special functions

The interacting system test may be enlarged to include testing of special functions such as direct digital control or supervisory (setpoint) control hardware, manual and automatic back-up stations, and fail-safe functions.

9 Recommended tests, environmental

Comprehensive environmental testing requires special equipment and procedures and is lengthy and expensive to perform. Since some system parameters may be affected by environmental changes, it is important that the user and vendor define the parameters and environments to be considered in testing. The actual environments the system may encounter and the parameters of importance in the anticipated system application are good guidelines for defining environmental test requirements.

The user should consider the cost as well as the advantages of each environmental test before negotiating these tests. It is not the intent of this standard to cover the complete spectrum of possible environmental tests.

9.1 Objective

The purpose of environmental testing is to verify contractual environmental specifications. Environmental testing may also reveal marginal components and faulty workmanship.

The following environmental factors are addressed in this section:

- 1) Temperature
- 2) Humidity
- 3) Input Power
- 4) Vibrations
- 5) Miscellaneous

9.2 Equipment to be tested

Only the equipment which the vendor supplies shall be tested unless otherwise negotiated by the vendor and user.¹

9.3 Testing procedures

The system can be tested in two basic configurations:

- 1) The total system
- 2) Each separate subsystem

However, there are many variations of these. A number of factors may influence the system configuration for testing:

- 1) Vendor manufacturing practices
- 2) User test requirements
- 3) Environmental specifications of each subsystem. Various subsystems may have different environmental specifications. When several subsystems are tested together, the environmental conditions shall not exceed the specifications of any of the subsystems.

The system test configuration should determine the tests performed on the system. The interacting system test may be used when testing the system as a unit and subsystem tests should be used when testing each subsystem separately.

Testing the system as a unit maybe the most straightforward. However, it is not as thorough as testing each subsystem separately. While the testing procedures for environmental testing may be the same as those defined in previous sections, the specifications may differ to account for the environmental conditions.

9.3.1 Temperature and humidity tests

The purpose of this test is to verify system operation at the specified temperature and humidity conditions.

Humidity testing should be combined with temperature testing in locations where the computer may be required to operate in a warm, humid atmosphere. Some system performance parameters are affected by humidity.

¹ It is felt that the order of importance in testing of subsystems is as follows:

- 1) CPU and Bulk Storage
- 2) Analog and Digital Input-Output (I/O)
- 3) Data Processing (DP) I/O

Each subsystem shall be operated in its normal enclosure. This test requires an environmental test chamber. If proper procedures are used, plastic tents can be used for these tests.

The following conditions are recommended for temperature tests:

- 1) Minimum specified temperature
- 2) Maximum specified temperature

When humidity tests are performed concurrently, the following conditions are recommended:

- 3) Minimum specified temperature and maximum humidity at that temperature
- 4) Maximum specified temperature and maximum humidity at that temperature²
- 5) Maximum specified humidity and maximum temperature at the humidity²

Specific test procedures shall be designed to avoid exceeding vendor specifications during the transition between environmental conditions. The equipment arrangement in the environmental chamber shall be such that any local extreme conditions are avoided. Sufficient time should be allowed between environmental changes to insure that a steady state has been reached.

9.3.2 Input power tests

The purpose of this test is to verify the ability of the system to compensate for input power variations to such degree that the system performance is not affected or impaired by such variations.

The power variations may include noise, superimposed pulses, interruptions, variations in voltage, frequency, and harmonic content. Testing procedures for determining effects of harmonic distortion, noise, and superimposed pulse are not included in this standard. [See C.1](#) for a discussion of these variations. Before specifications are considered for these tests, the user should determine the characteristics of his power source.

The following conditions are recommended for input power tests:

- 1) Maximum specified voltage and nominal frequency
- 2) Minimum specified voltage and nominal frequency
- 3) Maximum specified frequency and nominal voltage
- 4) Minimum specified frequency and nominal voltage
- 5) Input power interruptions of specified duration with nominal voltage and frequency before and after interruption

9.3.3 Vibration tests

Sophisticated vibration testing procedures are often impractical for use in routine testing of complete systems. Vendors usually perform vibration testing on new products as a product design verification test. Various unsophisticated techniques do exist, however, which are capable of revealing loose components and connections.

In cases where a specific vibration requirement must be satisfied by the equipment, special tests may be defined and performed. A further discussion of vibration and shock testing is in C.2.

² Conditions 4 and 5 may not be identical since maximum temperature and maximum humidity may not be allowed simultaneously by the system specification. If they are the same, Condition 5 is eliminated.

9.3.4 Miscellaneous environment

Consideration should be given to other environmental conditions under which the system is to operate. These might include: corrosive atmosphere, dust, salt water, spray, altitude, attitude, and radiation. A further discussion on corrosion is in C.3.

10 Documentation

10.1 Definition

The term "documentation" as used in this standard encompasses the evidence of tests performed on the hardware. It is not intended that the documentation cover test history beyond the scope of this Recommended Practice.

10.2 Types of documents

The documentation which may be contractually provided by the vendors is categorized into three types:

- 1) Type I
Statements or any evidence provided by the vendor that the hardware contracted on any given system has successfully passed the applicable tests. Type I documentation may consist of the system contract acceptance form, including applicable warranties, certificate of compliance, certificate of test performance, etc.
- 2) Type II
Itemized check list indicating contractual tests with a certification that each test has been successfully performed. Type II documentation may consist of a check list for categories of tests, such as environmental, input-output hardware, main frame performance, etc, or itemized lists for any or all of the applicable groups. It may also include a history of successful and unsuccessful tests if contractually required.
- 3) Type III
Individual numerical data, printouts, histograms, etc, compiled during the performance of contractual tests. Type III documentation shall be compiled in the format and according to the sequence of tests defined in the contractual agreement. It may also include a history of successful and unsuccessful tests if contractually required.

10.3 Extent of documentation

The documentation shall cover all applicable tests pertaining to the hardware within the scope of this standard in accordance with contractual agreements.

10.4 User - vendor agreement

The user and vendor shall negotiate the type and extent of documentation provided with the hardware as a part of the system contract. Additions, deletions, or other modifications to the originally-stipulated type and extent to documentation shall be renegotiated.

11 Glossary

This glossary of computer hardware testing terminology defines terms as used in this Recommended Practice. In order to standardize the use of terms, definitions have been taken from sources in common use, the primary source being ANSI standard X3.12 "Vocabulary for Information Processing." If a term is not listed in ANSI X3.12, other sources were used.

Terms in this glossary are listed in a single alphabetic sequence. The expression "see . . ." is used only for terms appearing in an inverted word order and serves to lead the user to the term where the definition appears.

11.1 Sources of definitions

The numbers appearing at the right of the definitions listed in this glossary designate the date of revision and the source of the definition. The first two numbers refer to the revision date — the last number identifies the source of the definition. A key to the source of definitions is given below:

- 0 - X3.12-1966 USA Standard, vocabulary for information processing.
- 1 - Executive Office of the President, Bureau of the Budget. Glossary, 1962.
- 2 - SAMA Standard PMC20C Draft No. 6, Measurement and Control Terminology, 1969.
- 3 - Foxboro, Glossary of Analog and Digital Process Control Terms, 1967.
- 4 - Control Data Corp. Glossary for Information Processing, 1966.
- 5 - General Electric, Glossary of Terms.
- 6 - IBM, Glossary for Information Processing, 1963.
- 7 - ISA Committee SP-55, Hardware Testing of Digital Process Computers.

11.2 Definitions

Access, Direct Storage (DSA): The procedure whereby data are transferred to or from storage essentially coincident with normal computer operation, without disturbing the central processing unit registers. 5/70-7

Access, random: 1) Pertaining to the process of obtaining data from, or placing data into, storage where the time required for such access is independent of the location of the data most recently obtained or placed in storage.

2) Pertaining to a storage device in which the access time is effectively independent of the location of the data. 1/70-0

Access, serial: Pertaining to the process of obtaining data from, or placing data into, storage when there is a sequential relation governing the access time to successive storage locations. 1/70-0

Accuracy: The degree of freedom from error, that is, the degree of conformity to truth or to a rule. Accuracy is contrasted with precision, e.g., four-place numerals are less precise than six-place numerals, nevertheless a properly computed four-place numeral might be more accurate than an improperly computed six-place numeral. 11/69-0

Accuracy, mean: Mean accuracy is precisely defined as $(100 - E) \% \text{ F.R.}$ Where the mean error E is expressed as a percentage of full range (F.R.). It is common practice, however, to equate

mean accuracy with the value of the mean error. That is, mean accuracy is commonly stated as 0.1% F.R. Whereas a more precise and acceptable statement is that mean accuracy is 99.9% F.R. 5/70-7

Accuracy, total: Total accuracy is precisely defined as $(100 - E_{\max}) \% \text{ F.S.}$ Where the maximum error $E_{\max}$ is expressed as a percentage of full scale value. It is a measurement of the worst case effect of all the errors present in the analog subsystem. 5/70-7

Alphanumeric: Pertaining to a character set that contains both letters and numerals, and usually other characters. Synonymous with Alphameric. 1/70-0

Analog: Pertaining to data in the form of continuously variable physical quantities. Contrast with digital. 1/70-0

Analog input: See Input, Analog.

Analog to Digital Converter (ADC): See Converter, Analog to Digital.

Analog output: See Output, analog.

Attenuation: (1) A decrease in signal magnitude between two points or between two frequencies.

(2) The reciprocal of gain, when the gain is less than one. 11/69-2

Block, data: A set of associated characters or words handled as a unit. 3/70-6

Binary: (1) Pertaining to a characteristic or property involving a selection, choice, or condition in which there are two possibilities.

(2) Pertaining to the numeration system with a radix of two. 1/70-0

Byte: A sequence of adjacent binary digits operated upon as a unit and usually shorter than a word. 4/70-0

Card hopper: See Hopper, card.

Card stacker: See Stacker, card.

Central processing unit: See Unit, Central Processing.

Chad: The piece of material removed when forming a hole or notch in a storage medium such as punched tape or punched cards. 1/70-0

Channel: (1) A path along which signals can be sent, e.g., data channel, output channel.

(2) The portion of a storage medium that is accessible to a given reading station.

(3) In communication, a means of one way transmission. Contrast with circuit.

(4) Sometime called a point. 2/70-0

Channel, input: The analog data path between the field wiring connector or termination strip and the analog-to-digital converter or other quantizing device used in the subsystem. In typical subsystems, this path may include a filter, an analog signal multiplexer, and one or more amplifiers. 5/70-7

Character: (1) One symbol of a set of elementary symbols such as those corresponding to the keys on a typewriter. The symbols usually include the decimal digits 0 through 9, the letters a through z, punctuation marks, operation symbols, and any other symbols which a computer may read, store, or write.

(2) The electrical, magnetic, or mechanical profile used to represent a character in a computer, and its various storage and peripheral devices. A character may be represented by a group of other elementary marks, such as bits or pulses.

Character embossing: A raising of the printing medium surface within the perimeter of a printer character caused by the impact of a type element against printing medium. 11/70-7

Check, parity: A check that tests whether the number of ones (or zeros) in an array of binary digits is odd or even. Synonymous with odd-even check. 1/70-0

Check, validity: A check based upon known limits or upon given information or computer results, e.g., a calendar month will not be numbered-greater than 12, and a week will not have more than 168 hours.

Clock, real time: A clock which indicates the passage of actual time, in contrast to a fictitious time set up by the computer program; such as, elapsed time in the flight of a missile, where in a 60-second trajectory is computed in 200 actual milliseconds, or a 0.1 second interval is integrated in 100 actual microseconds. 11/69-1

Code, Hollerith: A widely used system of encoding alphanumeric information onto cards, hence Hollerith cards are synonymous with punch cards. 5/70-1

Command: (1) An electronic pulse, signal or set of signals to start, stop or continue some operation. It is incorrect to use command as a synonym for instruction.

(2) The portion of an instruction word which specifies the operation to be performed.

Common Mode Rejection (CMR): The ability of a circuit to discriminate against common mode voltage, usually expressed as a ratio or in decibels. 5/70-3

Common Mode Voltage (CMV): See Voltage, Common Mode.

Contact input: See Input, contact.

Contact output: See Output, contact.

Control, direct multiplex: A control means using hardware, a computer program, or both, to directly interleave or simultaneously receive or transmit two or more signals on a single channel. 5/70-7

Converter, Analog to Digital (ADC): An instrument used to convert analog signals to digital coded values which are proportional to the analog input voltages. 11/70-7

Converter, Digital to Analog (DAC): An instrument which converts digital information into analog signals which are proportional to the numerical value of the digital information. 5/70-7

Counter, input: The storage and buffer device between an external pulse source and the computer; e.g., a real time clock or some other totalizing unit. 5/70-7

CPU: The abbreviation for central processing unit. See Unit, Central Processing. 2/70-7

cross-talk: The unwanted energy transferred from one circuit, called the "disturbing" circuit, to another circuit, called the "disturbed" circuit. 11/69-0

Cursor: A symbol used in the operation of keyboard-video displays to indicate on the display screen the physical location of the next character to be entered.

Cycle stealing: A control feature which delays execution of a program to allow an I/O device to communicate with main storage without changing the logical condition of the CPU. 5/70-7

Data packing: To compress several items of data in a storage medium in such a way that the individual items can later be recovered. 5/70-7

Data Processing (DP): Pertaining to any operation or combination of operations on data. 5/70-0

Data unpacking: The process of recovering individual items of data from packed information. 5/70-7

Deletion punch: A record elimination feature used on paper tape I/O devices to cause all tape channels to be punched. 5/70-7

Digit: A character used to represent one of the non-negative integers smaller than the radix, e.g., in decimal notation, one of the characters 0 to 9. 1/70-0

Digital: Pertaining to data in the form of digits. Contrast with analog. 1/70-0

Digital input: See Input, digital.

Digital output: See Output, digital.

Digital to Analog Converter (DAC): See Converter, digital to analog.

Direct Storage Access (DSA): See Access, direct storage.

Direct Storage Access Channel (DSAC): A channel for direct access to storage. See Access, Direct Storage. Also, See Channel. 5/70-7

Direct multiplex control: See Control, direct multiplex.

Droop rate: The rate at which the voltage output of a storage device decays. 5/70-7

Duplex, full: Method of operation of a communication circuit where each end can simultaneously transmit and receive. 5/70-5

Duplex, half: Permits one direction, electrical communication between stations. Technical arrangements may permit operation in either direction but not simultaneously. 5/70-5

Edit: To rearrange data or information. Editing may involve the deletion of unwanted data, the selection of pertinent data, the application of format techniques, the insertion of symbols such as page numbers and typewriter characters, the application of standard processes such as zero suppression, and the testing of data for reasonableness and proper range. Editing may sometimes be distinguished between input edit (rearrangement of source data) and output edit (preparation of table formats).

Error, maximum: The maximum error $E_{\max}$ of the analog subsystem is defined as the deviation between the true value of the input signal and the particular output reading within the distribution of output readings furthest displaced from the true value. 5/70-7

Executive: Short for executive routine. See Routine, executive.

Full duplex: See Duplex, full.

Full Range (F.R.): The algebraic difference between the minimum and maximum values for which a device is specified. 5/70-7

Full Scale (F.S.): The maximum absolute value for which a device is specified. 5/70-7

Half Duplex: See Duplex, half.

Harmonic distortion: Distortion characterized by the appearance in the output of harmonics other than the fundamental component when the input wave is sinusoidal. 5/70-7

Hollerith code: See Code, Hollerith.

Hopper, card: A device that holds cards and makes them available to a card feed mechanism. Synonymous with input magazine. 5/70-0

Input: (1) The data to be processed.

(2) The state or sequence of states occurring on a specified input channel.

(3) The device or collective set of devices used for bringing data into another device.

(4) A channel for impressing a state on a device or logic element.

(5) The process of transferring data from an external storage to an internal storage. 1/70-0

Input, analog: Information or data in analog form transferred or to be transferred from an external device into the computer system. 11/69-7

Input, contact: A digital input generated by operating an external contact. 5/70-7

Input, digital: Information or data in digital form transferred or to be transferred from an external device into the computer system. 11/69-7

Input channel: See Channel, input.

Input counter: See Counter, input.

Input-output, data processing: (1) A general term for the equipment used to communicate with a computer.

(2) The data involved in such communication.

(3) The media carrying the data for input-output operations on data. 5/70-7

Input resistance: See Resistance, input.

Input signal: See Signal, input.

Interface: A common boundary between automatic data processing systems or parts of a single system. 11/69-1

Interlock: To arrange the control of machines or devices so that their operation is interdependent in order to assure their proper coordination. 11/69-1

Interrupt: Suspension of the execution of a routine as a result of a hardware or program generated signal.

Interrupt, process: Those interrupts available for connection to the user supplied equipment. Synonymous with external interrupt. 5/70-7

Linearity: The closeness to which a curve approximates a straight line. 11/69-2

Load: (1) To put data into a register or storage.

(2) To put a magnetic tape onto a tape drive, or to put cards into a card reader.

(3) An electrical device connected to the output terminals.

(4) To connect a signal receiving device to the output terminals of a signal source. 5/70-7

Main storage: Usually the fastest storage device of a computer and the one from which instructions are executed. Contrasted with storage, auxiliary. 5/70-1

Mark sensing: See Sensing, mark.

Maximum, error: See Error, maximum.

Mean accuracy: See Accuracy, mean.

Mean error (E): The mean error is defined as the deviation between the mean value of a statistically significant number of output readings and the true value of the input signal. The mean error is expressed as a percentage of the full range (F.R.). 5/70-7

Mode: (1) A computer system of data representation, e.g., the binary mode.

(2) A selected method of computer operation. 11/69-1

Modem: A term used in reference to a device used in data transmission; a contraction of "modulator-demodulator." The term may be used with two different meanings:

(1) The modulator and the demodulator of a modem are associated at the same end of a circuit.

(2) The modulator and the demodulator of a modem are associated at the opposite ends to form a channel. 11/69-5

Multiplexer: A device which interleaves or simultaneously transmits two or more messages or signals on a single channel. 11/70-7

Noise: (1) An unwanted component of a signal or variable which obscures the information content.

(2) Random variations of one or more characteristics of any entity, such as voltage, current, or data.

(3) A random signal of known statistical properties of amplitude, distribution, and spectral density.

(4) Loosely, any disturbance tending to interfere with the normal operation of a device or system.

Normal mode rejection: The ability of a circuit to discriminate against normal mode voltage, usually expressed as a ratio or in decibels. 5/70-7

Normal mode voltage: See Voltage, normal mode. 5/70-7

Output, Analog: Nominally pertains to output of data in the form of continuously variable physical quantities as contrasted with digital output. Most analog output subsystems utilize digital to analog converters which provide a finite number of output levels and only approximate a continuous variable. 5/70-7

Output, contact: A digital output generated by operating a contact. 5/70-7

Output, digital: Pertaining to the output of data in the form of digits. Contrast with analog output. 11/69-7

Overload recovery: Refers to an effect caused by an analog signal input greater than that for which the feedback capacity of an amplifier can compensate. The result is a loss of feedback control by the amplifier and thereby requiring some recovery time after the overload is removed. 5/70-7

Parallel: (1) Pertaining to the simultaneity of two or more processes.

(2) Pertaining to the simultaneity of two or more similar or identical processes.

(3) Pertaining to the simultaneous processing of the individual parts of a whole, such as the bits of a character and the characters of a word, using separate facilities for the various parts. 1/70-0

Parity check: See Check, parity.

Points: Synonymous with channel. 5/70-7

Polling: The act of requesting a station to send data in switching networks. 5/70-7

Process interrupt: See Interrupt, process.

Quantizing interval: The smallest change in the input signal to a quantizing device which causes a change in the quantized representation of the input signal. 5/70-7

Random access: See Access, random.

Real time clock: See Clock, real time.

Record: (1) A group of related facts or fields of information treated as a unit, thus a listing of information, usually in printed or printable form.

(2) To put data into a storage device. 11/69-1

Reference ground: A datum level from which input-output signals are measured. 5/70-7

Registration: The accurate positioning relative to a reference. 1/70-0

Repeatability: Normally considered to be a measurement of performance made over a very short period of time; a period short enough so that gain and offset instabilities of system components are of no significance. In terms of the distribution of readings, it is a measure of the maximum deviation of the readings from the mean value of the distribution. 5/70-7

Resistance, input: The resistance appearing at the input terminal of a device. 11/69-7

Resolution: A measure of the smallest input change which can be detected (not necessarily measured) at the output of the system. 11/70-7

Routine: A set of instructions arranged in proper sequence to cause a computer to perform a desired task. 1/70-0

Routine, executive: A routine that controls the execution of other routines. Synonymous with supervisory routine. 1/70-0

Sample and Hold: A device which senses and stores the value of an analog signal units subsequently updated. 11/70-4

Sensing, mark: A technique for detecting special pencil marks entered in special places on a punch card and automatically translating the marks into punched holes. 5/70-1

Serial: (1) Pertaining to the time-sequencing of two or more processes.

(2) Pertaining to the time-sequencing of two or more similar or identical processes, using the same facilities for the successive processes.

(3) Pertaining to the time-sequential processing of the individual parts of a whole, such as the bits of a character or the characters of a word, using the same facilities for successive parts. 1/70-0

Serial access: See Access, serial.

Settling time: See Time, settling.

Signal, input: A signal applied to a device, element, or system. 5/70-3

Spread: In some performance measures, the total dispersion or spread of readings required. The spread S may be defined as,

$$S = R_1 + R_2$$

where R_1 and R_2 refer to the maximum deviation of the readings from either side of the mean value of the distribution. See Repeatability. 5/70-7

Stability: A measure of the ability of a device to maintain constant values for one or more parameters describing its operation. 11/70-7

Stacker, card: An output device that accumulates punched cards in a deck. 5/70-4

Statistically significant number of readings: A statistically significant number of readings is a sample whose statistics closely approximate the true statistics of the parameter under consideration. That is, increasing the number of readings or repeatedly performing the data collection procedure will not result in substantially different calculated statistical parameters such as the mean and deviation. 5/70-7

Storage, main: See Main storage.

Submultiplexer boundary: See discussion under Submultiplexer group.

Submultiplexer group: In analog signal multiplexer construction, it is common to separate the analog input channels into groups of, typically, 4 to 64 channels. The outputs of the channels included in any single group are bussed together and provide an input to another (second level) multiplexer, the output of which is commonly connected to the subsystem amplifier or analog to digital converter. The group of input channels connected together to form a single group in such

a multi-level multiplexer is called a submultiplexer group in this standard. The submultiplexer boundary for such a group is the electrical boundary defined by the second level multiplexer switching device connected to the common output of the submultiplexer group. 5/70-7

Subsystem: Any assemblage of components which operates as a part of a system, and which is collectively capable of performing a task within, and as defined by, that system. 2/70-4

System: (1) An organized collection of parts united by regulated interaction.

(2) An organized collection of men, machines, and methods required to accomplish a specific objective. 2/70-0

Time, settling: The time required, following the initiation of a specified stimulus to a system, for the output to enter and remain within a specified narrow band centered on its steady-state value. 11/69-2

Timer, watchdog: An electronic interval timer which will generate an interrupt unless periodically recycled by a computer. It is used to detect program stall or hardware failure conditions. 11/70-7

Total accuracy: See Accuracy, total.

Track: The portion of a moving storage medium, such as a drum, tape, or disk, that is accessible to a given reading head position. 1/70-0

True value: The true value of a quantity is the value which would be measured with a perfect (i.e., error-free) measurement instrument. From a practical standpoint, the true value is often considered to be the value of a quantity measured by comparison to a primary standard such as those maintained by the National Bureau of Standards. For the purposes of this standard, the recommended true value is the value of a quantity obtained by comparison with a defined reference quantity. This reference quantity to which measurements are to be referred in the tests described in this standard shall be specified by the vendor or agreed upon by the vendor and user. 5/70-7

Unit, Central Processing (CPU): The unit of a computing system that includes the circuits controlling the interpretation and execution of instructions. 2/70-0

Validity check: See Check, validity.

Value referred to the input: The value obtained by dividing an output value by the nominal gain of the subsystem. 5/70-7

Voltage, Common Mode (CMV): That amount of voltage of the same polarity and phase common to both input lines. Common mode voltage can be caused by magnetic induction, capacitive coupling, and resistive coupling. 5/70-7

Voltage, normal mode: The actual voltage difference between input signal lines. 5/70-7

Watchdog timer: See Timer, watchdog.

Appendix A Analog input subsystem accuracy

A major criterion employed in evaluating the performance of analog input subsystems is the system accuracy. All system purchasers, users, and vendors discuss system accuracy, yet very seldom do two people agree on an exact definition of the term. Since a widely-accepted standard terminology is not available for this parameter, it is recommended that this standard be interpreted in terms of definitions provided in this appendix unless specific exceptions are agreed upon by the user and vendor.

A.1 Introduction

A precise definition of accuracy is that it is a measure of the degree of freedom from error; that is, the degree of conformity to a true value. Therefore, for a specific analog input signal, the subsystem should produce an output which is the true value in order to be 100 percent accurate. However, in practice, measurements are subject to fixed and statistical variations. Thus, repeated readings taken using the same analog input source may not be precisely the same. Rather, certain measurements may occur more frequently than others. If the number of measurements of each value is plotted as a function of the reading, a distribution similar to that illustrated in [Figure A.1](#) might be obtained. The discrete histogram derived from the data is often approximated by a smooth distribution curve as indicated by the dotted line in the figure. The mean (or average) value $\bar{x}$ for all of the measured values is indicated in the figure, together with the true value x_t . The mean error is defined as the difference between the true value and the mean value.

If all of the error sources within the system are perfectly random, the measurements assume a "normal" or "Gaussian" distribution and the distribution curve has a "bell shape" similar to [Figure A.2](#). Distributions of actual analog input subsystem measurements may be non-Gaussian and may be lopsided or skewed as shown in [Figure A.1](#). Occasionally, the distribution may even contain multiple peaks. These characteristics are caused by systematic or periodic errors and the tendencies of some system components to recognize particular values rather than others.

A.2 System accuracy components

The contributions to the total mean error from which system accuracy is determined is subdivided into four component areas:

- 1) Fixed Errors
- 2) Repeatability
- 3) Variable Errors
- 4) Operational Errors

A.2.1 Fixed errors

Fixed errors result from factors such as gain inaccuracies, zero offsets, and errors in the reference supply of the analog-to-digital converter. Most systems have gain and offset adjustments but, since the adjustments have a finite resolution, the error generally is not reduced to zero. Note that these errors are independent of time and temperature.

A requirement in the testing of the analog input subsystem is that the gain and offset adjustments be made prior to testing so that these errors may be minimized.

A.2.2 Repeatability

Repeatability is normally considered to be a measurement of noise performance made over a specified period of time (a period short enough such that instabilities of system components which are time and temperature dependent are of no significance).

Noise errors are created within all system components and are also induced into the system by external means. Noise in an analog input subsystem can be categorized as:

- 1) Random noise (or white noise) whose power is uniformly distributed in the frequency domain.
- 2) Systematic noise that exhibits definite power peaks at specific frequencies.

Random noise is typically generated within the system by certain solid-state devices, etc.

Systematic noise is created by choppers and similar devices and is often induced into analog subsystems from periodic sources such as the clock in the digital system.

R_1 and R_2 in [Figure A.1](#) represent a measure of the variation of readings taken using the same analog input source. R_1 is the variation of readings greater than the mean value, while R_2 is the variation of readings less than the mean value. Spread (S) refers to the total dispersion of readings.

There is a small but finite probability that any given sample of readings for the same analog input source may contain values far outside the remainder of the distribution. Such "wild" readings may be due to a variety of causes including the random nature of noise existing in the system. If the number of such readings is small, it is considered reasonable to exclude them in determining the maximum and minimum bounds on the distribution. A commonly used technique, and the one recommended for use in this standard, is to define the specification and measurement of repeatability on a statistically significant basis. This basis uses the $\pm 3 \sigma$ deviation of a normal distribution, where σ is the standard deviation, as the criterion for defining repeatability. For a normal distribution, 99.7 percent of the samples are within this $\pm 3 \sigma$ range.

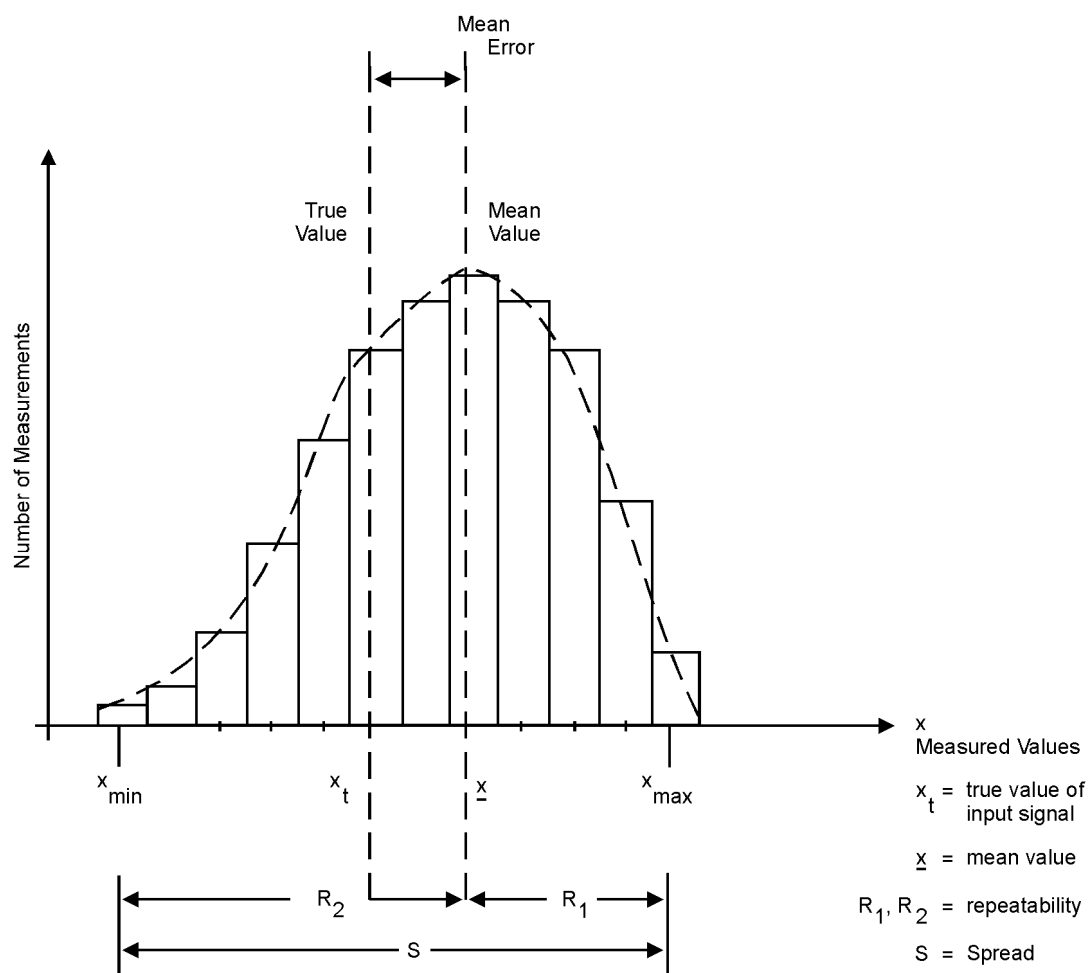


Figure A.1 — Typical analog input subsystem histogram

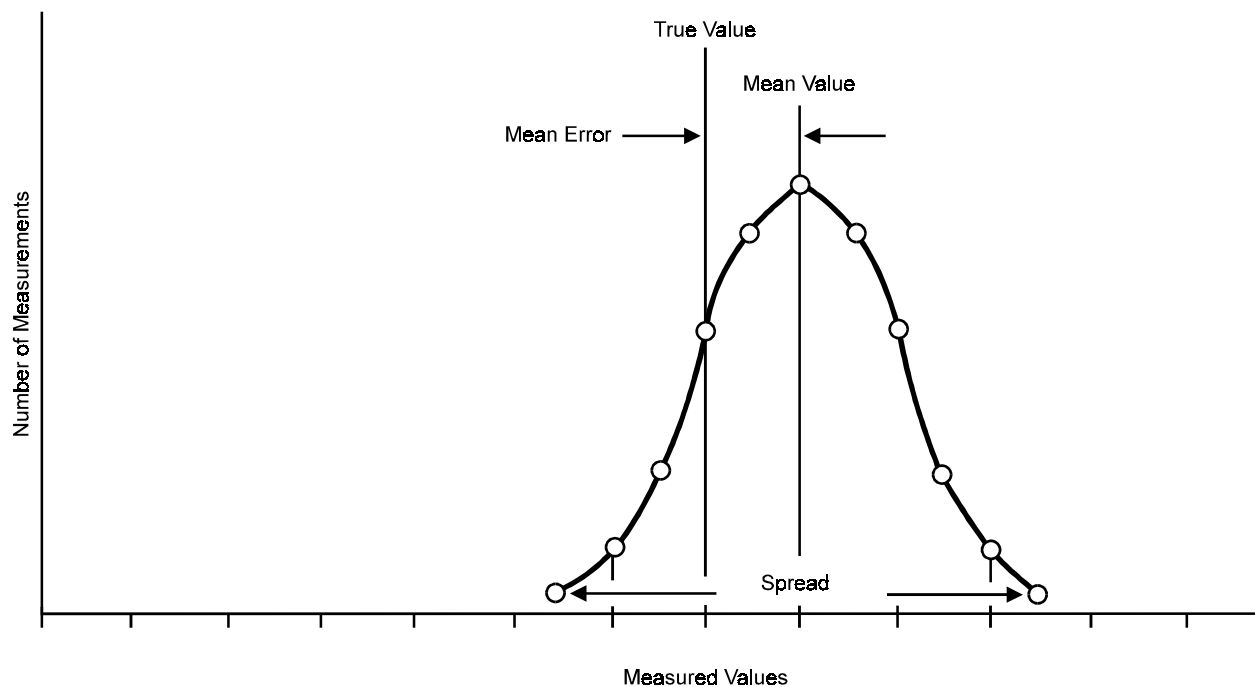


Figure A.2 — Histogram indicating normal distribution

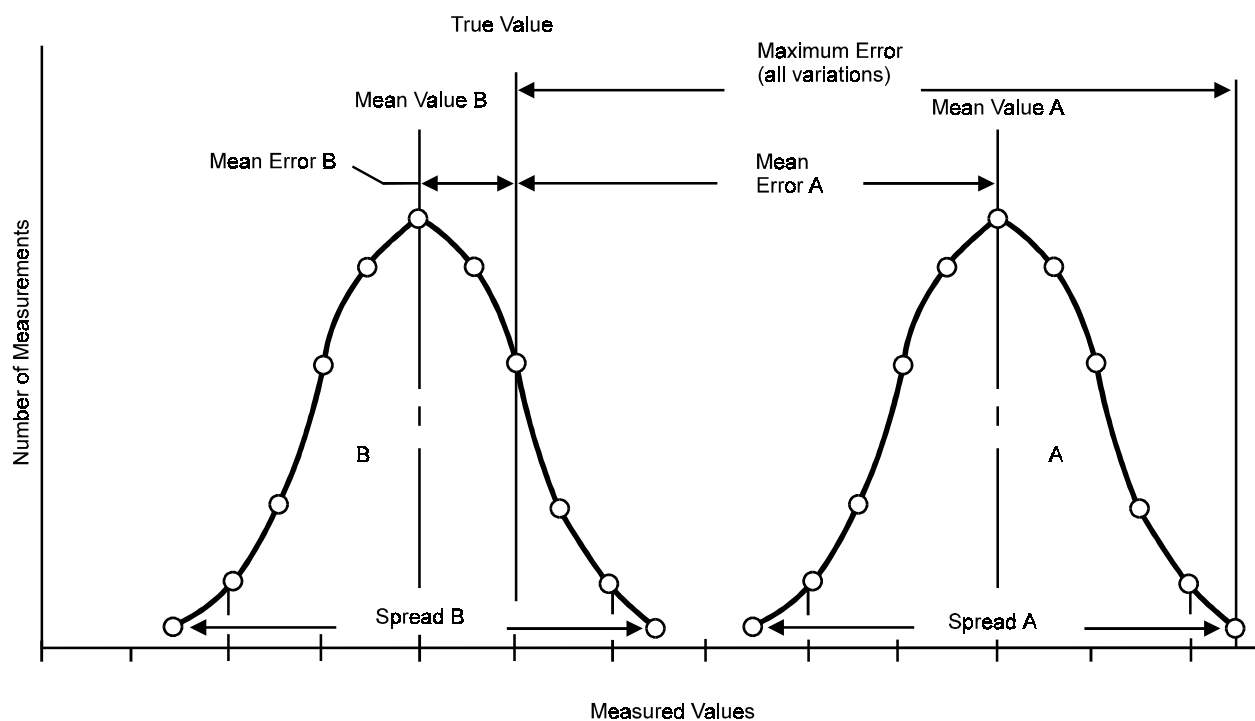


Figure A.3 — Histogram - time and temperature variations included

The use of the 99.7 percent or, as it is commonly called, the 3 σ confidence level has the following interpretation and effect in measuring the repeatability of an analog input subsystem:

There are 99.7 percent of N samples in the distribution which will be within the deviation from the mean defined by the repeatability specification.

In terms of evaluating the performance of an actual system, this method of specifying repeatability means that 0.3 percent of the readings in a sample of N readings may be disregarded. The readings to be disregarded are those farthest from the measured mean.

A.2.3 Variable errors

Variable errors are errors that change as a function of time and temperature. At a given point in time and at a given temperature they are zero. These errors may be caused by the following:

- 1) Gain instability with time
- 2) Gain temperature coefficient
- 3) Zero offset instability (drift with time)
- 4) Zero offset temperature coefficient

The mean values in [Figures A.1 and A.2](#) are subject to variation with time and temperature. Accordingly, the error between the mean value and the true value varies similarly. [Figure A.3](#) depicts two distribution curves for the same input source. Curve B represents readings taken at a different time or temperature than the readings taken for Curve A.

Variable errors are not measured as part of the analog input subsystem accuracy tests, since these are made at constant temperatures over a short time duration. They may be included, however, within the interacting system and environmental tests.

A.2.4 Operational errors

Operational errors are errors whose magnitudes are determined by the manner in which the system is employed. Typical errors in this group are:

- 1) Common mode voltage errors
- 2) Duty cycle errors

The latter includes both errors which are dependent on signal source and system environment.

A.3 Accuracy calculations

A method of deriving "mean" and "total accuracy" is given in Sections A.3.2 and A.3.3. In the strictest sense, evaluating the "absolute accuracy" of a system requires the use of the National Bureau of Standards primary voltage reference as an input signal source. The system vendor and user usually have available a standard cell (possibly traceable to an NBS reference) and bridge-type potentiometer to measure the analog input signal. Generally these devices are precise enough to use in determining mean and total accuracy.

A.3.1 Terminology

A.3.1.1 Statistically significant number of readings

The term, "statistically significant number of readings," is an important factor which must be understood before one can interpret the accuracy calculations properly. A statistically significant number of readings is a sample whose statistics closely approximate the true statistics of the parameter under consideration. That is, increasing the number of readings or repeatedly performing the data collection procedure will not result in substantially different calculated statistical measures such as the mean and deviation.

The following formula is provided as a guideline for determining a statistically significant number of readings:

$$N \geq (R/\delta E)^2$$

where

R = repeatability specification in percent F.R.

E = mean error specification in percent F.R.

δ = allowable fractional error in the calculated mean of the N readings (a value of 0.1 is suggested for current subsystems)

This guideline provides a probability in excess of 99 percent that the calculated value of mean error is within $\pm\delta E$ percent F.R. of the true mean error if the distribution of readings is statistically normal. The use of this guideline should be tempered by experience gained in testing the subsystem.

Example:

Specification:

Mean error = 0.10 percent F.R.

Repeatability = 0.24 percent F.R. (99.7 percent probability)

Select $\delta = 0.1$ so that the mean will be determined within limits of 0.1 (0.1) = ± 0.01 percent F.R.

Then $N \geq 0.24/(0.1 \times 0.1))^2 = (24)^2 = 576$

A.3.1.2 Use of "Full Range" and "Full Scale"

For purposes of this standard, certain calculations such as those for accuracy and repeatability, are expressed as a percentage of full range rather than full scale. Full range is defined as the algebraic difference between the minimum and maximum values to which the Analog Input or Output subsystem is specified. Full scale is the maximum absolute value (for each polarity) to which the subsystem is specified.

Several examples are listed in [Table A.1](#).

Table A.1 — Full range-full scale examples

Specification	Bipolar/Unipolar	Full Range Value	Full Scale Value
$\pm 50\text{mV}$	Bipolar	100mV	50mV (Positive polarity) 50mV (Negative polarity)
0 to +50mV	Unipolar	50mV	50mV
-10 to +40mV	Bipolar	50mV	40mV (Positive polarity) 10mV (Negative polarity)

A.3.2 Mean accuracy calculation

Mean accuracy A is precisely defined as (100 – E) percent F.R. where the mean error E is expressed as a percentage of full range value. It has been common practice, however, to equate mean accuracy with the value of the mean error. For example, mean accuracy is commonly stated as 0.1 percent F.R. whereas a more precise and acceptable statement is that the mean accuracy is 99.9 percent F.R.

The mean error of the subsystem is defined as the deviation between the mean value of a statistically significant number of output readings $\bar{x}$ and the true value of the input signal x_t . Figures A.1 through A.3 indicate this relationship.

The mean value of the output readings referred-to-the-input (RTI) is calculated for each input signal value according to the formula:

$$\bar{x} = \frac{\sum_{i=1}^N x_i}{N}$$

where

N = total number of readings excluding overloads

x_i = value of the i-th output reading RTI

$\bar{x}$ = mean value of the N output readings RTI

The indicated summation excludes overload readings since these are indeterminate.

Mean error E is calculated as a percentage of full range according to the formula:

$$E = \left| \frac{\bar{x} - x_t}{x_{F.R.}} \right| \times 100$$

where

x_t = true value of the input signal

$x_{F.R.}$ = nominal full range value of the input signal

Mean accuracy A as a percentage of full range is calculated as follows:

$$A = (100 - E)$$

Example:

Normal full range value ($x_{F.R.}$) = 10.00mV

Normal full scale value = 5.000mV

True value of input signal (x_t) = + 2.500mV

Output readings referred to input (RTI). One thousand readings taken.

Output Value RTI mV		Number of Occurrences	
	+ 2.475	2	
	2.480	0	
x_{min}	2.485	2	
	2.490	15	R_2
	2.495	60	
x_t	2.500	260	
$\bar{x}$	2.505	410	
	2.510	210	R_1
	2.515	30	
x_{max}	2.520	10	
x_{mr}	2.525	1	
		1000	total

Since 0.3 percent of all readings taken can be discarded (see A.2.2), the two readings of 2.475 mV and the one at 2.525 mV can be omitted from the calculations.

The mean value of output readings $\bar{x}$ is calculated as 2.505 mV. The mean error E in percent F.R. is

$$E = .005 / 10 \times 100 = 0.05 \text{ percent F.R.}$$

$$A = (100 - E) = 99.95 \text{ percent F.R.}$$

A.3.3 Total accuracy

Total Accuracy A_{tot} is precisely defined as $(100 - E_{max})$ percent F.R. where the maximum error E_{max} is expressed as a percentage of full range value. It is a measurement of the worst case effect of all the errors present in the analog subsystem other than effects due to external factors such as common mode voltage or operational factors such as cross-talk. (See A.2)

The maximum error of the subsystem is defined as the deviation between the true value of the input signal and the particular output reading within the distribution of output readings furthest displaced from the true value.

E_{max} is calculated as a percentage of full range value according to the formula:

$$E_{max} = \left| \frac{x_t - x_{mr}}{x_{F.R.}} \right| \times 100$$

where

x_{mr} = the particular output reading furthest displaced from the true value after statistically insignificant readings have been discarded.

x_t and $x_{F.R.}$ have the same definition as in A.3.2

Total Accuracy (A_{tot}) as a percentage of full range is calculated as follows:

$$A_{\text{tot}} = (100 - E_{\text{max}})$$

Example:

In the example of A.3.2, $x_{\text{mr}} = 2.520$ mV.

$$E_{\text{max}} = \frac{0.020}{10} \times 100 = 0.2 \text{ percent F.R.}$$

$$A_{\text{tot}} = (100 - E_{\text{max}}) = 99.8 \text{ percent F.R.}$$

When accuracy measurements are made over long periods of time or temperature variations, the mean of the distribution is likely to vary. [Figure A.3](#) indicates this variation, where curve "A" represents the distribution at one time and temperature, and curve "B" at another. The total accuracy calculation must reflect the effective output reading furthest displaced from the true value during the specified time and temperature interval. Note that the spread may remain the same even though the total accuracy changes.

A.4 Linearity error

The procedure described is based on the calculation of the deviation of the mean value of the readings from a least-square-fit linear transfer function defined by:

$$y = a + bx_t$$

where

y = expected value of the mean output value RTI for an input signal x_t

x_t = true value of the input signal

a, b = constants calculated using the "least square error" routine for a "best fit" transfer function

The technique of the least squares is a widely used method of fitting a straight line to a series of data. This method gives the best fit to the data since it makes the sum of the squared deviations from the line of best fit, smaller than they would be from any other straight line. On the average, the deviations below this line equal those above the line.

The least-square-fit function is not constrained to pass through the origin. The calculation is valid for unipolar and bipolar subsystems.

The values of constants a and b as determined below ensure that the sum of the squares of the deviations will be a minimum.

$$a = \frac{(\sum x_t)(\sum x_t x) - (\sum x_t^2)(\sum x)}{(\sum x_t)^2 - n(\sum x_t^2)}$$

$$b = \frac{(\sum x_t)(\sum x) - n(\sum x_t x)}{(\sum x_t)^2 - n(\sum x_t^2)}$$

where

$\bar{x}$ = the mean value of the output readings referred to the input (RTI) calculated for each input signal x_t (See A.3.1)

n = Total number of input signal values utilized in the mean accuracy test.

The summations are taken over the total number of input signal values.

The linearity error expressed as a percentage of full range is based on the maximum value of the difference between y and $\bar{x}$ or

$$L = \frac{\bar{x} - y}{x_{F.R. \max}} \times 100$$

Further information regarding the development of these equations can be secured from the referenced texts. See Table A.2 for an example.

Table A.2 — Linearity Example

Input Signal True Value RTI	Mean Output Value RTI	$x_t \bar{x}$	x_t^2	Least-Square-Fit Transfer Function	Linearity Error (% F.R.)
x_t	$\bar{x}$			$y = a + bx_t$	$L = \frac{ \bar{x} - y }{x_{F.R.}} \times 100$
–100.0 mv	–100.0 mv	10000	10000	–100.577	0.289
–80.0	–80.5	6440	6400	–80.447	0.026
–60.0	–61.0	3660	3600	–60.317	0.342
–40.0	–40.3	1612	1600	–40.187	0.057
–20.0	–20.2	404	400	–20.057	0.072
0	–0.1	0	0	0.0727	0.014
+20.0	+20.1	402	400	20.203	0.052
+40.0	+40.8	1632	1600	40.333	0.234
+60.0	+61.2	3672	3600	60.463	0.369*
+80.0	+80.8	6464	6400	80.593	0.104
+100.0	+100.0	10000	10000	100.723	0.362
$\Sigma x_t = 0.0$	$\Sigma \bar{x} = +0.8$	$\Sigma x_t \bar{x} = 44286$	$\Sigma x_t^2 = 44000$		
$n = 11$ $a = \frac{(0.0)(44286) - 44000 \times 0.8}{0 - 11 \times 44000} = 0.0727$ $b = \frac{0 \times 0.8 - 11 \times 44286}{-11 \times 44000} = 1.0065$ $x_{F.R.} = 200\text{mv}$					

* $L_{\max} = 0.369\%$

Appendix B Interacting systems

B.1 Typical subroutines executed under interrupt control

Typical subroutines include those to:

- 1) Schedule the subsystem programs on a periodic, aperiodic, or on a demand basis.
- 2) Resolve conflicts between common input-output device demands.
- 3) Transfer control to subroutines on a pre-established priority basis.
- 4) Provide real-time clock servicing.
- 5) Reset the watchdog timer.

B.2 Test duration factors

The test duration required to provide reasonable assurance that interacting system effects will be detected varies significantly depending upon a number of factors. In negotiating the length of this test, some of the factors that should be considered are:

- 1) Complexity of the system.
- 2) Subsystem noise sensitivity.
- 3) Relative speed of the various subsystems being tested.
- 4) Characteristics of the program being used to exercise the system (such as degree of overlapped operation, capability of running accelerated tests, and synchronous versus asynchronous operation).
- 5) Time dependent factors such as changes in temperature or power source characteristics which may be encountered during the test.

B.3 Histogram plot

An optional qualitative diagnostic aid is to use the histogram data for characterizing non-random biasing of the analog conversion. This, however, since it is qualitative, does not constitute a pass-fail criterion. The method uses a plotting of the histogram data on probability graph paper (such as K&E No.359-23). Random distribution is indicated if the resulting curve is basically linear.

Appendix C Environment

C.1 Input power

Power interruption of the order of a few milliseconds provides a measure of the energy storage within the system. This stored energy provides some system protection to power disturbances such as noise, switching transients, lightning, momentary frequency shifts, and harmonic distortion. Therefore, the observed system performance during power interruption of this kind provides a relative indication of its ability to withstand certain power disturbances.

Energy in the form of short pulses, may be coupled into the computer system from the primary power source. For example, transients due to lightning strikes often take this form. The power interruption test does not provide an indication of the effect of this type of disturbance. However, more knowledge and test data are required before standard test procedures can be established.

C.2 Vibration testing

The primary benefit of routine vibration testing is often the identification of loose components and connections. In line with this objective, a wide range of test methods and equipment may be used with satisfactory results. Routine vibration testing of complete computer systems is normally impractical because of the equipment required. However, since most problems due to vibration occur at various connector interfaces and in backpanel wiring, vibration testing of backpanels and connectors would be useful.

Vibration testing generally falls into three categories: sinusoidal vibration, acoustical noise, and shock.

Sinusoidal vibration test equipment for small subassemblies is readily available. This test equipment adequately vibrates three or four 19" wide printed circuit card rows as an assembly. During vibration, functional electrical testing of the subassembly complete with all electronics is desirable if a meaningful test can be designed. If this procedure is not practical, testing continuity of all connected pins and insulation of all nonconnected pins with an automatic testing device during vibration may be a meaningful procedure.

Shock testing may be performed using calibrated shock apparatus or by the simple expedient of tapping components with an insulated device. In spite of the apparent crudeness of the latter method, it is meaningful for all connectors and plugs in a system to be firmly rapped during the system test. Care should be exercised so as not to damage equipment when this type of test is being performed.

Large-scale vibration and acoustical noise testing of a total computer system is difficult to define and requires specialized equipment. Normally, this type of test is performed to qualify equipment which must withstand extreme environmental conditions such as in military and aerospace applications. When tests such as these are required, reference may be made to appropriate military and aerospace specifications on vibration and acoustical testing.

C.3 Corrosion

Corrosive atmosphere testing techniques have not been sufficiently developed to define meaningful tests. However, serious consideration should be given to the atmosphere in which the computer system is to operate. The presence of corrosive elements such as Cl_2 , H_2S , SO_2 , and SO_3 can cause damage to computer equipment. Combinations of these elements and humidity often accelerate such damage.

References

- 1) Bennett, C. A. and Franklin, N. L.; "Statistical Analysis in Chemistry and the Chemical Industry"; New York; John Wiley & Sons, Inc., 1967; pp. 222-224.
- 2) Hoel, P. G.; "Introduction to Mathematical Statistics"; Third Edition; New York; John Wiley & Sons, Inc., 1962; pp. 168-172.

Index

A	Section
Accuracy	5.1, 7.1, A.3
Analog Tests	6.1, 6.3.3, 7.3.2
Counting	5.3.1.5
Pulse Count	5.3.2.6
Timing	5.3.2.5
Addressing	5.3.1.1, 5.3.2.1, 6.3.1, 7.1, 7.3.1
Analog Inputs	6.0, 8.2, 8.3.1
AC Normal Mode Rejection	6.1, 6.3.7
Accuracy Test	6.1, 6.3.3
Addressing Test	6.1, 6.3.1
Common Mode Cross-talk Test	6.1, 6.3.11
Common Mode Rejection	6.1, 6.3.6
DC Cross-talk	6.1, 6.3.10
Gain Changing Cross-talk	6.1, 6.3.12
Input Overload	6.1, 6.3.9
Input Resistance	6.1, 6.3.8
Linearity	6.1, 6.3.4
Sampling Rate	6.1, 6.3.2
Analog Outputs	7.0, 8.2, 8.3.5
Accuracy	7.1, 7.3.2
Addressing Tests	7.1, 7.3.1
Cross-talk	7.1, 7.3.7
AC	7.3.7.2
DC	7.3.7.1
Droop Rate	7.1, 7.3.8
Noise	7.1, 7.3.5
Output Capability	7.1, 7.3.3
Settling Time	7.1, 7.3.6
Analog to Digital Converter (ADC)	6.3.2, A.2.1
Arithmetic and Control Logic	3.3.1, 8.3.8
Instruction Execution	3.3.1.2
Instruction Load	3.3.1.1
 B	
Binary-Coded Decimal Subsystem	7.3.2.2
Binary-Code Subsystem	7.3.2.1
Bipolar	6.3.4, A.3.1.2
Byte Manipulation	3.3.2.2
 C	
Capacitive Loading	7.1, 7.3.4

	Section
Card Readers and Punches Tests	4.3.1
Card Transport	4.3.1.4
Interlocks	4.3.1.1
Operational Switches, Keys	4.3.1.2
Punch Operations	4.3.1.3
Read Operations	4.3.1.3
Central Processing Unit (CPU)	3.0
Subsystem to be Tested	3.2
Test Methods and Procedures	3.3
Channel	3.3.3, 6.3.1, 6.3.7, 6.3.8, 6.3.12, 7.3, 7.3.6, 8.3.1
Common-Mode Noise Rejection, (CMR)	See Common-Mode Rejection
Common-Mode Rejection, (CMR)	5.3.1.4, 6.3.6
Common Mode Voltage, (CMV)	6.3.6, 6.3.11
Confidence Level	A.2.2
Consoles	8.3.13
Costs	2.8
CPU	See Central Processor
Cross-talk	6.1, 7.1, 7.3.7.2
Common Mode	6.3.11
DC Cross-talk	6.3.10, 7.3.7.1
Error	7.3.7.1
Gain Changing	6.3.12
Current Output Channel	7.3.3.2
Current Regulation	7.3.3.2
Customer-Vendor Agreement	2.4, 10.4
 D	
Data Collection Terminals Tests	4.3.8, 8.2, 8.3.14
Interlocks	4.3.8.1
Operational Switches, Keys	4.3.8.2
Receive Data	4.3.8.3
Transmit Data	4.3.8.3
Data Modems Tests	4.3.9, 8.2, 8.3.14
Control, Interchange Circuits	4.3.9.4
Equalization	4.3.9.2
Performance Characteristics	4.3.9.3
Signal Conditioning	4.3.9.1
Digital I/O	5.0, 8.2, 8.3.2
Disk Storage Device Tests	4.3.3, 8.2
Access Operation	4.3.3.3
Interlocks	4.3.3.1
Operational Switches, Keys	4.3.3.2
Read Data Transfer	4.3.3.3
Write Data Transfer	4.3.3.3

	Section
Documentation	10.0
Extent	10.3
Types	10.2
Droop Rate	7.1, 7.3.8
Drum Storage Device Test	4.3.4, 8.2
Interlocks	4.3.4.1
Operational Switches, Keys	4.3.4.2
Read Data Transfer	4.3.4.3
Write Data Transfer	4.3.4.3
 E	
Environmental Testing	9.0
AC Power	9.3.2, C.1
Altitude	9.3.4
Attitude	9.3.4
Corrosion	9.3.4, C.3
Dust	9.3.4
Frequency	9.3.2, C.1
Harmonic Distortion	9.3.2, 9.3.4, C.1
Humidity	9.3.1
Radiation	9.3.4
Salt Water Spray	9.3.4
Temperature	9.3.1
Vibration	9.3.3, C.2
Equipment to be tested	3.2, 4.2, 5.2, 6.2, 7.2, 8.2, 9.2
Executive Program	8.3
External Synchronization	6.3.13, 7.3.9
 F	
Factors to be considered	1.0, 2.0
Filters	6.3.7
Full Range	A.3.1.2
Full Scale	A.3.1.2
 G	
Gain, Multiple	6.3.3.3, 6.3.9, 6.3.12
Glossary	11.0
 H	
Hardware Interrupts	3.3.4
Acknowledge	3.3.4.1
Auto Restart	3.3.4.5
Enable-Disable	3.3.4.2
Miscellaneous	3.3.4.6
Multi-Level	3.3.4.3
Power-Fail	3.3.4.4
Humidity	6.3, 7.3

I	Section
Input, Resistance	6.1, 6.3.8
Inputs	5.3.1
Contact	5.3.1.2.1
Delay	5.3.1.3
Digital	5.3.1, 8.2
Pulse	5.3.1.5, 8.2, 8.3.3
Voltage	5.3.1.2.2
Inputs Analog	See Analog Inputs
Interacting Systems Tests	8.0, APP B
Purpose	8.1
Subsystem to be tested	8.2
Interrupts	3.3.4, 5.3.1.6, 8.3.11
I/O	4.0, 5.0
I/O Adapters	3.3.2
Byte Manipulation	3.3.2.2
Device Address	3.3.2.1
Device Ready	3.3.2.3
Error Checks	3.3.2.4
I/O Channels	2.5, 6.3.8, 6.3.9, 6.3.10, 6.3.11, 6.3.12
I/O Direct Storage Access Channel	3.3.3
Termination	3.3.3.2
Typical Functions	3.3.3.1
 K	
Keyboards and Consoles Test	4.3.10
Keys and Switches	4.3.10.1, 4.3.10.2
Lamps, Neon Indicators	4.3.10.3
 L	
Linearity	6.3.4
Error	6.3.4, A.4
 M	
Magnetic Tape Device Tests	4.3.5
Interlocks	4.3.5.1
Operational Switches, Keys	4.3.5.2
Read Data Transfer	4.3.5.3
Tape Transport	4.3.5.4
Write Data Transfer	4.3.5.3
Main Storage	3.3.6, 8.2, 8.3.7
Addressing	3.3.6.1
Circuit Load Test	3.3.6.3
Storage Protect	3.3.6.4
Worse Case Pattern Test	3.3.6.2
Mean Accuracy Test	6.3.3, 6.3.3.1, 6.3.3.3, 7.3.2, 7.3.2.1, A.3.2

	Section
Mean Error	6.3.12, 7.3.2.1, 7.3.2.2, A.3.2
Mean Value	7.3.2.1, 7.3.2.2, 7.3.7.1, A.3.2
Maximum Error	A.3.3
Multiplex	6.3.2
N	
Noise	7.1, 7.3.5, 7.3.7.2, 9.3.2, A.2.2, C.1
Noise, Common-Mode, (CMN)	See Common-Mode
Noise, Normal-Mode, (NMN)	See Normal-Mode
Noise Rejection	5.3.1.4
Normal-Mode Noise, (NMN)	See Noise
Normal-Mode Rejection, (NMR)	5.3.1.4, 6.3.7
O	
Open Circuit Detection	6.3.13
Output Capability	7.1, 7.3.3
Outputs	5.3.2
Contact	5.3.2
Delay	5.3.2.4
Digital	5.3.2, 8.3.4
Pulse	5.3.2.6
Timed	5.3.2.5
Voltage	5.3.2.3
Oscillations	7.3.4, 7.3.7.2
Overload Channel	6.3.9
Overload Recovering Effect	6.3.9
Overvoltage Protection	6.3.13
Overvoltage Testing	5.3.1.6
P	
Paper Tape Readers or Punchers Test	4.3.2, 8.2, 8.3.9
Interlocks	4.3.2.1
Operational Switches, Keys	4.3.2.2
Punch Operation	4.3.2.3
Read Operation	4.3.2.3
Tape Transport	4.3.2.4
Power Failure	7.3.9
Power Failure Status	5.3.2.2
Repeatability	6.3.5, A.2.2, A.3.1.1
S	
Sample-and-Hold Amplifiers	6.3.13
Sample-and-Hold	7.1, 7.3.8
Sampling Rate	6.1, 6.3.2
Settling Time	7.1, 7.3.6
Signal Conditioning	6.3.7

	Section
Signal Level	5.3.1.2, 5.3.2.3
Signal Source	7.3
Single-Gain Subsystem	6.3.3.1, 6.3.3.2
Source Resistance	6.3.3.1, 6.3.3.2, 6.3.8, 6.3.9
Spread	6.3.6, 6.3.7
Statistical Significant No. Reading	6.3.3.1, 6.3.6, 6.3.7, 6.3.8, 6.3.9, 6.3.12, A.3.1.1
Storage Protection	8.3.15
Submultiplexer Boundary	6.3.6
Submultiplexer Group	6.3.9, 6.3.11
Subsystems	8.2
Analog Input	8.3.1
Analog Output	8.3.5
Bulk Storage	8.3.6
Card Readers, Punches	8.3.9
Consoles	8.3.13
Core Storage	8.3.7
CPU	8.3.8
Digital Input	8.3.2
Digital Output	8.3.4
External Interrupt	8.3.11
Modems	8.3.14
Paper Tape Readers, Punches	8.3.9
Pulse Input	8.3.3
Terminals	8.3.14
Timers	8.3.12
Typers and Line Printers	8.3.10
System Accuracy	App A
Accuracy Calculations	A.3
Common Mode Voltage Errors	A.2.4
Distribution	A.1
Duty Cycle Errors	A.2.4
Fixed Errors	A.2
Gain and Offset Adjustments	A.2.1
Gain Instability	A.2.3
Gaussian Distributions	A.1
Histogram	A.1
Mean Error	A.1, A.3.2
Noise	A.2.2
Operational Errors	A.2, A.2.4
Random Noise	A.2.2
Repeatability	A.2
Statistical Variations	A.1
Systematic Noise	A.2.2
True Value	A.1
Variable Errors	A.2, A.2.3

	Section
Wild Readings	A.2.2
Zero Offset Instability	A.2.3
Zero Offset Temperature Coefficient	A.2.3
T	
Temperature	6.3, 6.3.3, 7.3, 9.3.1, A.2.3, A.3.3
Termination Strip	5.2, 6.2, 7.2
Test Equipment	2.7, 6.3
Time	6.3.3, A.2.3, A.3.3
Timers	3.3.5, 8.2, 8.3.12
Interval	3.3.5.1
Real Time	3.3.5.3
Watchdog	3.3.5.2
Total Accuracy	6.3.3.2, 6.3.3.3, A.3.3
Maximum Error	6.3.3.2, A.3.3
Mean Accuracy A	6.3.3.1, A.3.2
Mean Accuracy Test	6.3.3.1
Mean Error E	6.3.3.1, A.3.2
Mean Value x	6.3.3.1, A.3.2
Repeatability	6.1, 6.3.5, A.2.2
Typers and Line Printers Tests	4.3.6, 8.2, 8.3.10
Carriage, Forms Transport	4.3.6.4
Interlocks	4.3.6.1
Operational Switches, Keys	4.3.6.2
Print Operations	4.3.6.3
Print Quality	4.3.6.3
U	
Unipolar Subsystems	6.3.3.1, 6.3.4, A.3.1, A.3.1.2
User-Vendor Agreement	10.4
V	
Vibration	9.3.3, C.2
Video Display Stations Tests	4.3.7
Image Characteristics	4.3.7.2
Indicators	4.3.7.1
Operational Keys, Switches	4.3.7.1
Voltage Output Channel	7.3.3.1
Voltage Regulation	7.3.3.1
W	
Warm-up Time	6.3, 7.3
Watchdog Timer	3.3.5.2

Developing and promulgating technically sound consensus standards, recommended practices, and technical reports is one of ISA's primary goals. To achieve this goal the Standards and Practices Department relies on the technical expertise and efforts of volunteer committee members, chairmen, and reviewers.

ISA is an American National Standards Institute (ANSI) accredited organization. ISA administers United States Technical Advisory Groups (USTAGs) and provides secretariat support for International Electrotechnical Commission (IEC) and International Organization for Standardization (ISO) committees that develop process measurement and control standards. To obtain additional information on the Society's standards program, please write:

ISA
Attn: Standards Department
67 Alexander Drive
P.O. Box 12277
Research Triangle Park, NC 27709

ISBN: 0-87664-392-6